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FIG. 1

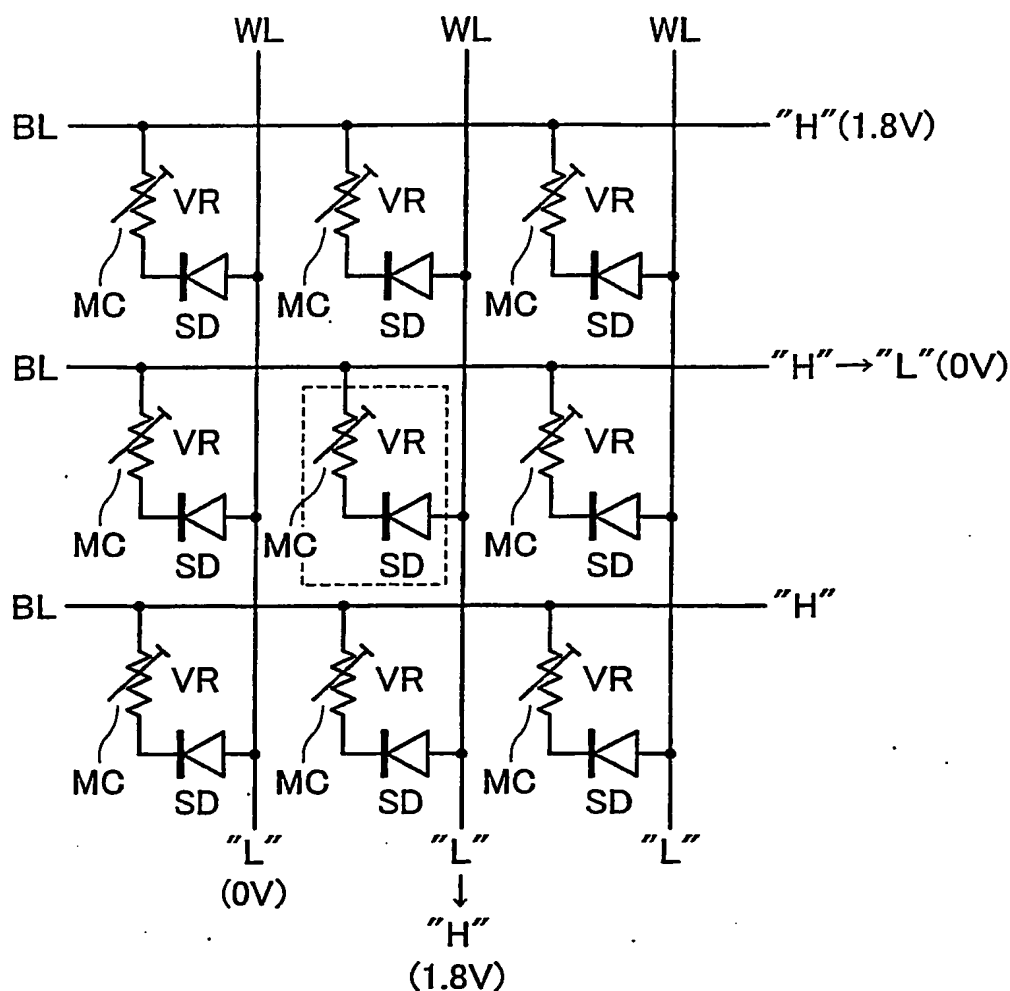


FIG. 2

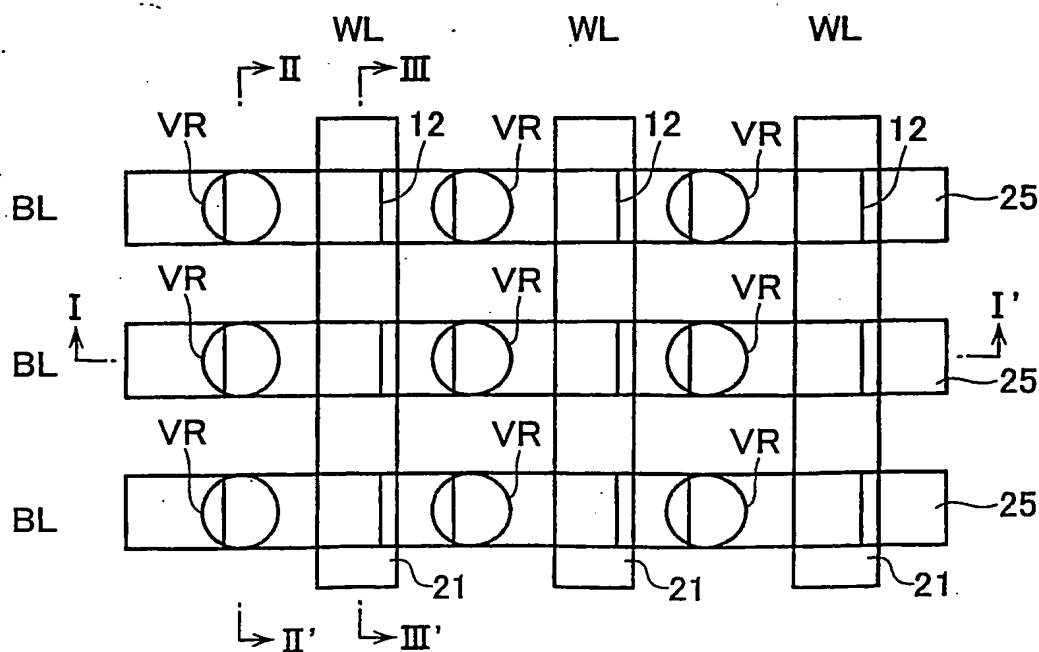


FIG. 3A

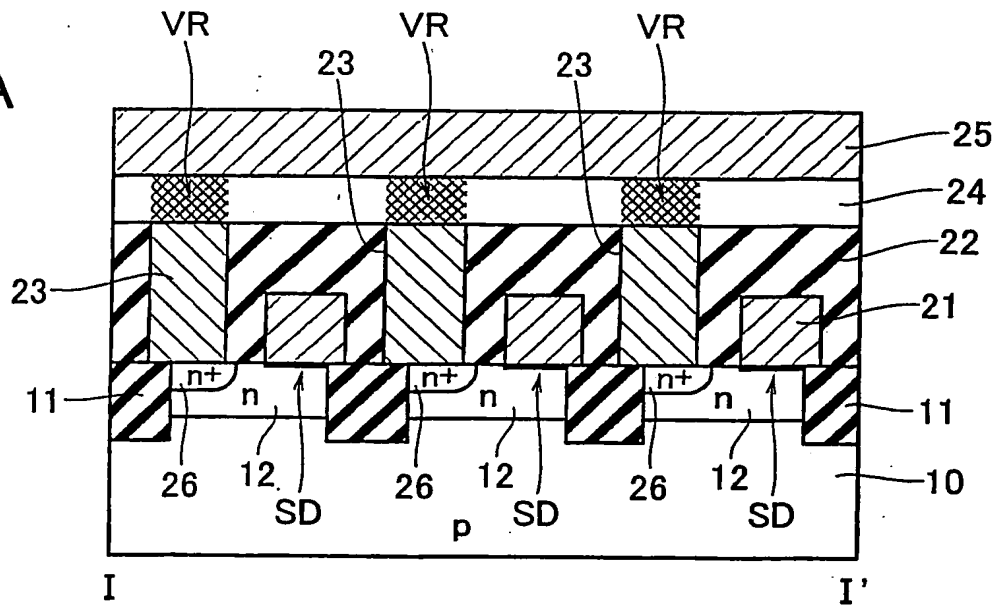


FIG. 3B

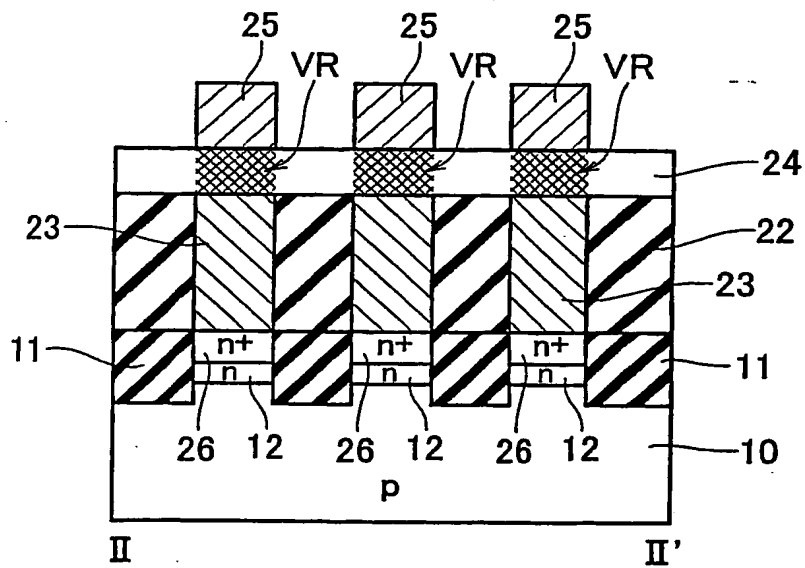


FIG. 3C

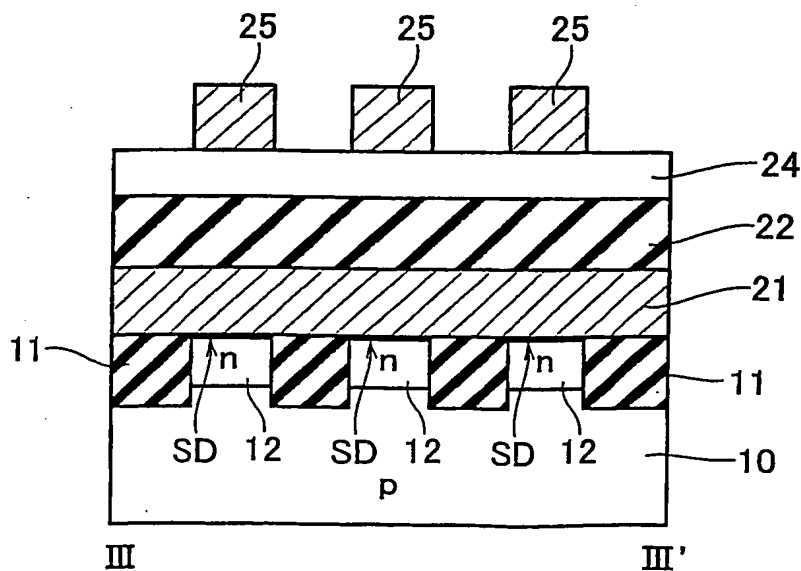


FIG. 4

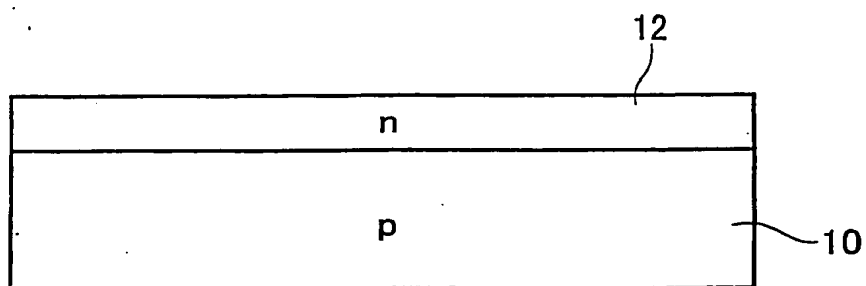


FIG. 5

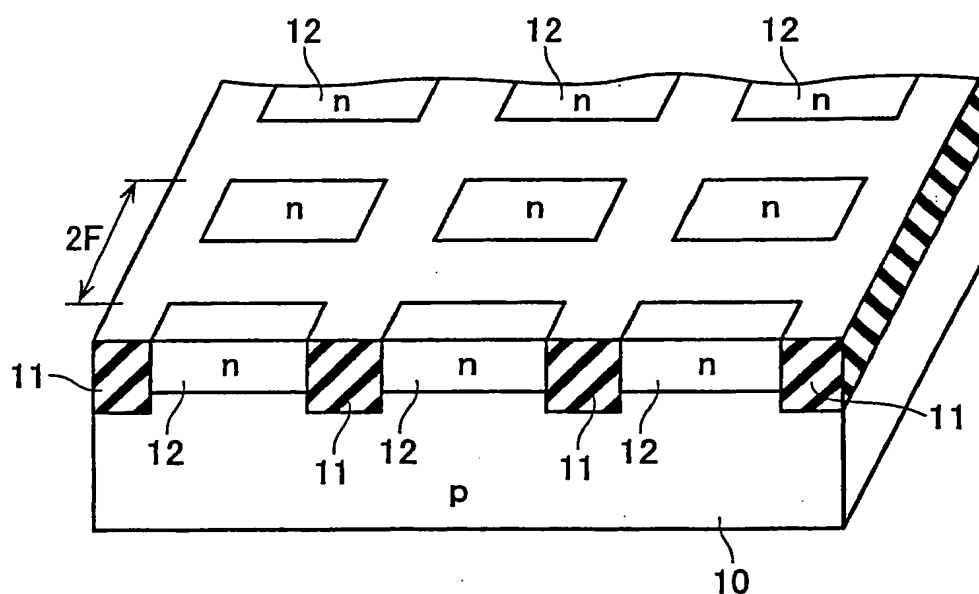


FIG. 6

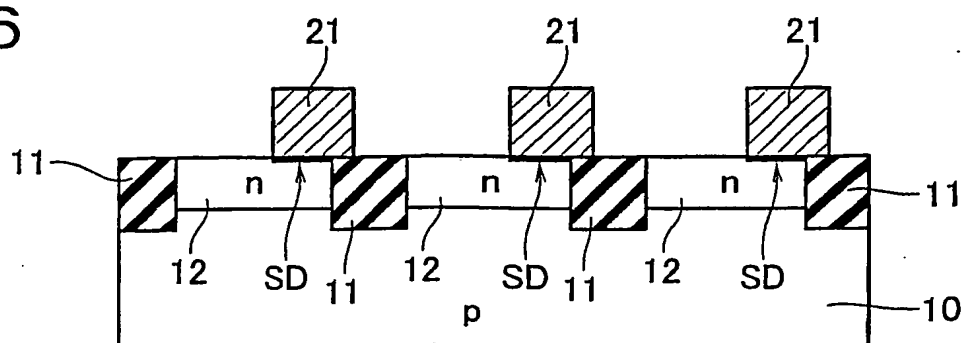


FIG. 7

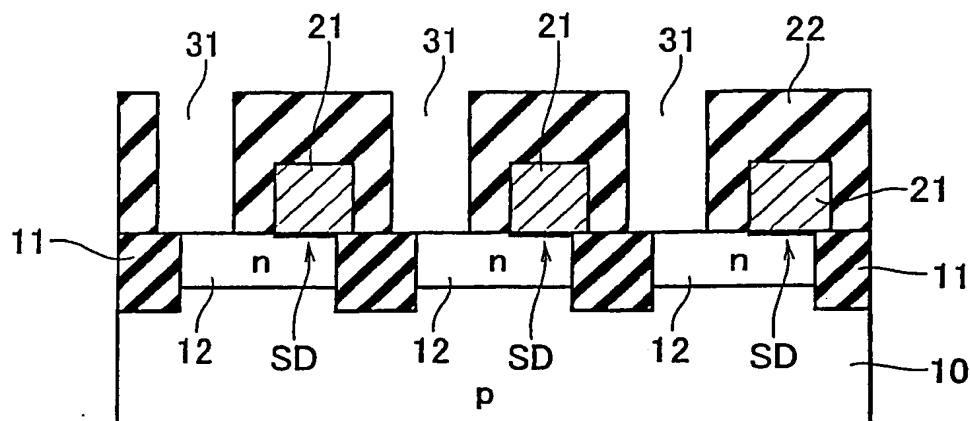


FIG. 8

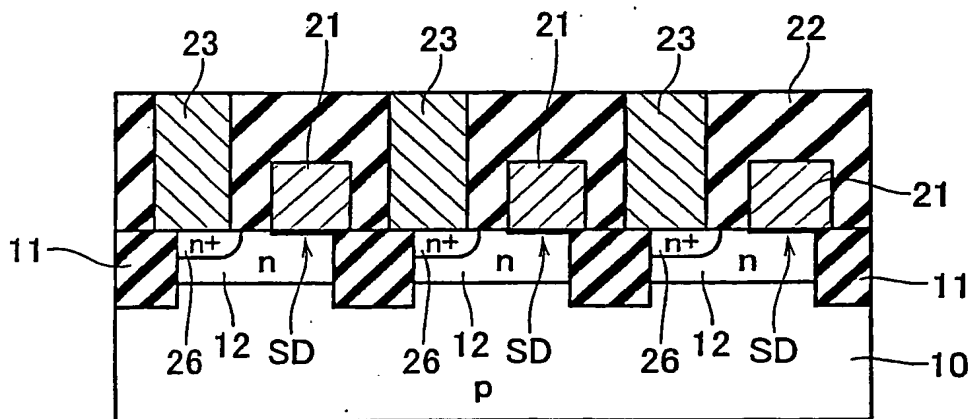
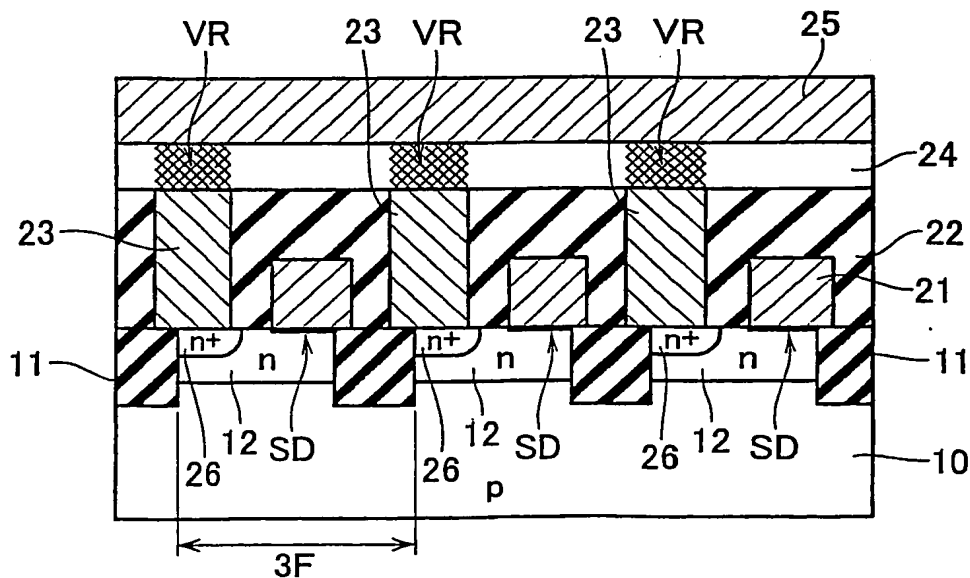


FIG. 9





[illegible]

A cross-sectional view of a semiconductor device, labeled 10, showing a repeating unit structure. The device consists of several layers and regions. At the top is a layer 25 with diagonal hatching. Below it is a layer 24 with a cross-hatch pattern. Underneath is a layer 22 with diagonal hatching. The bottom-most layer is 11, which contains regions labeled  $n$  and  $n^+$ . The  $n$  regions are separated by  $n^+$  regions. The  $n$  regions are further divided into segments labeled SD, 12, and 26. Above the  $n$  regions are three vertical structures, each consisting of a central region 21 (with diagonal hatching) and side regions 23 (with diagonal hatching). These structures are separated by regions 12 and 26. The top of these structures is labeled VR. The entire structure is labeled 10 at the bottom right.

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FIG. 14

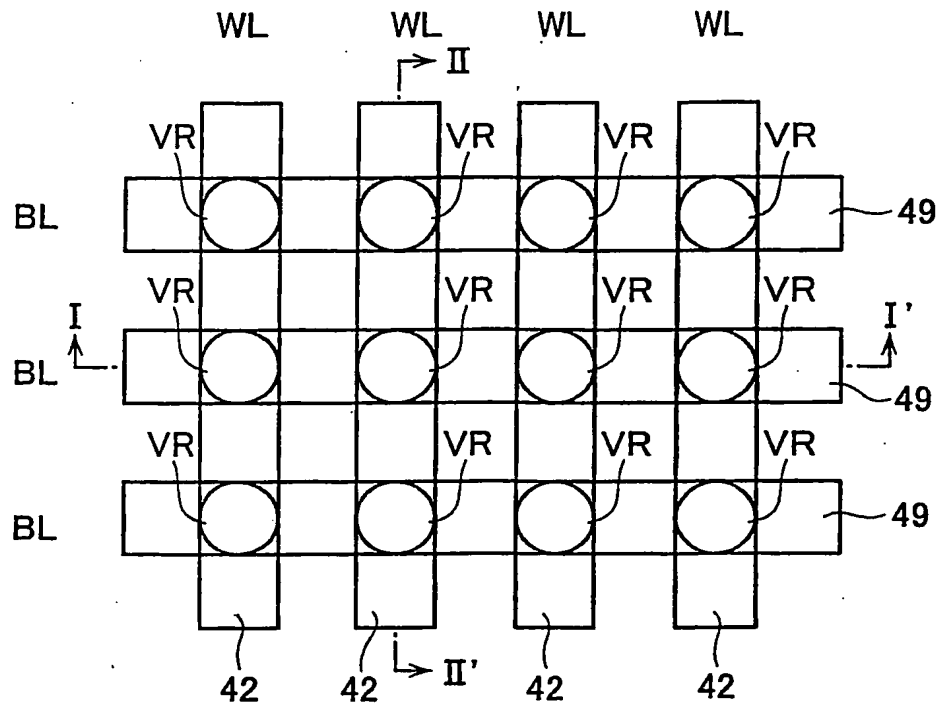
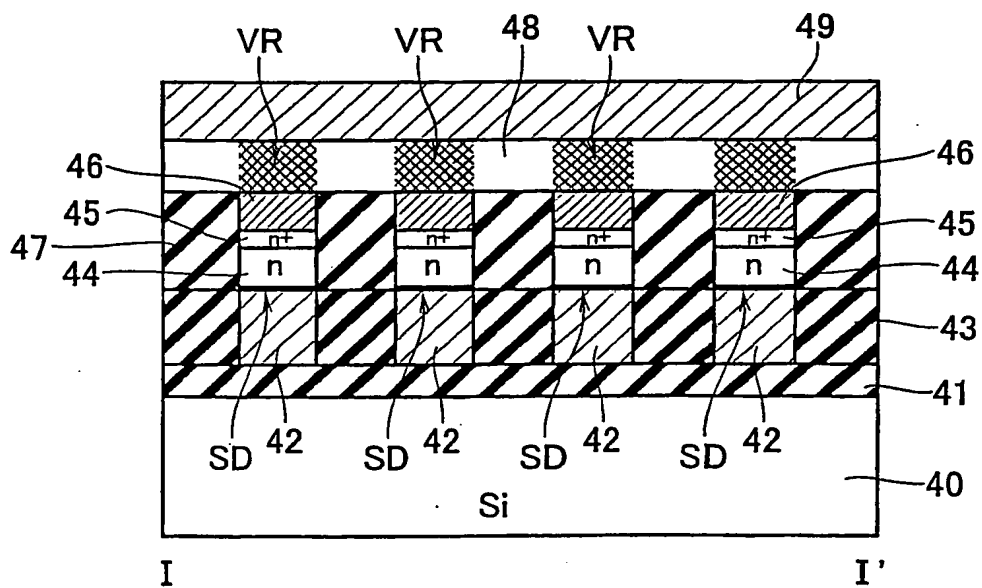


FIG. 15A



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FIG. 15B

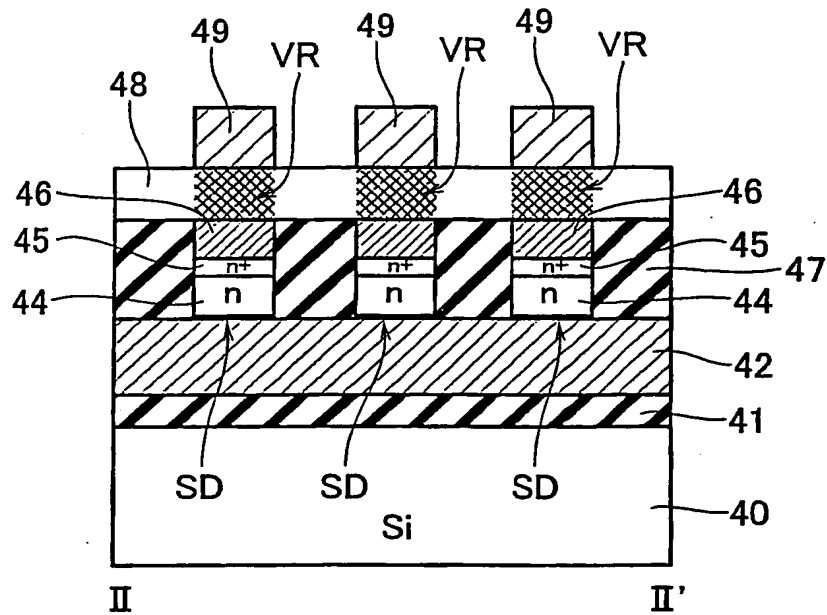


FIG. 16

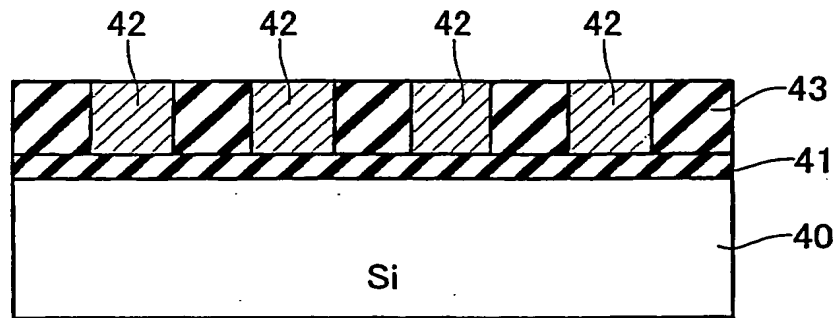


FIG. 17

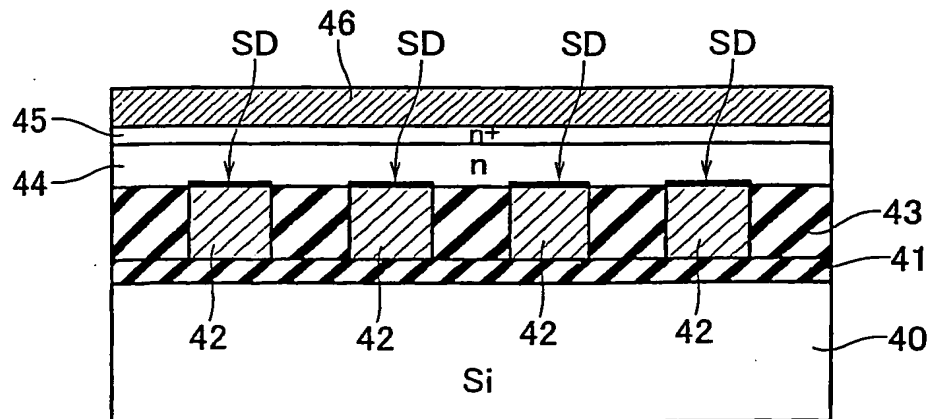




FIG. 18

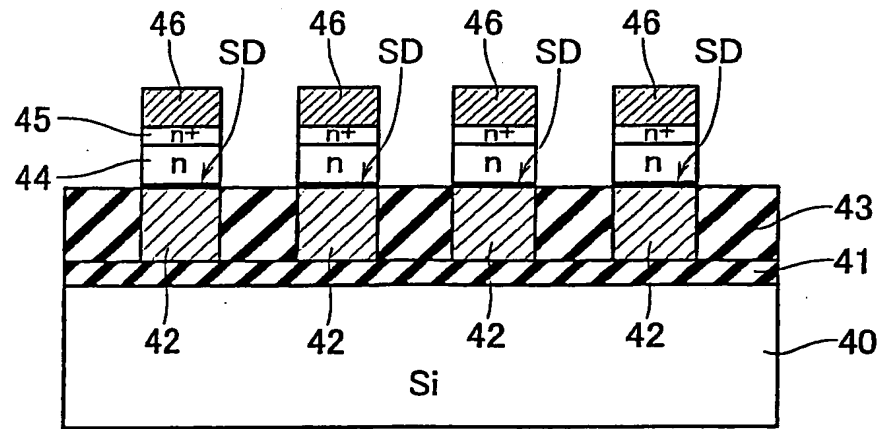
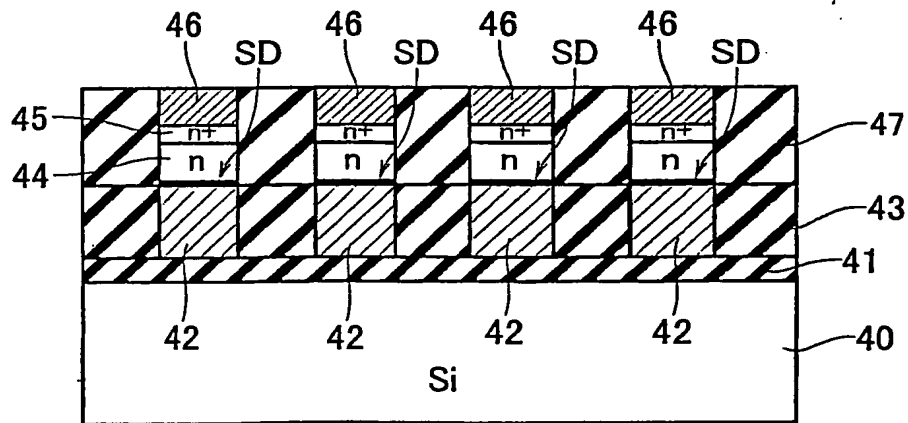
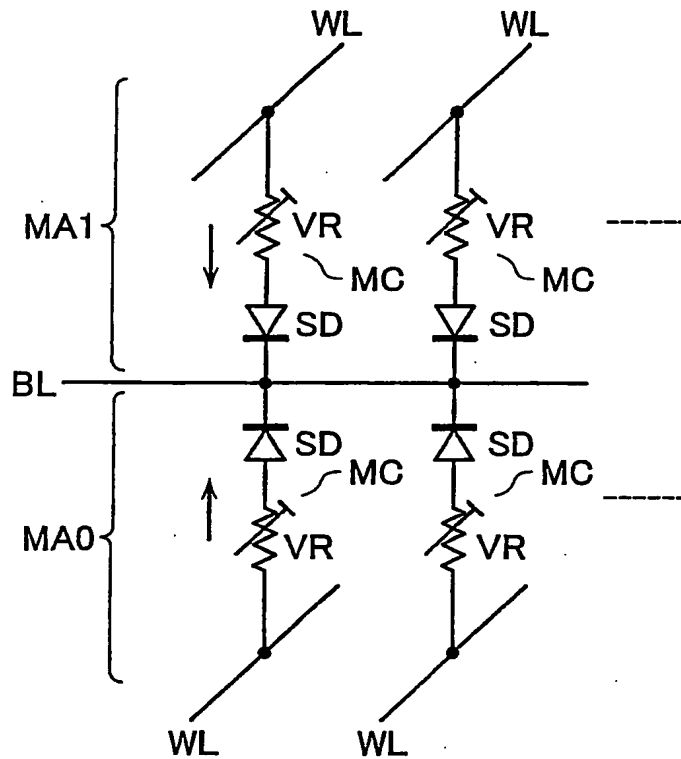


FIG. 19



The diagram illustrates a 1T1R1C1S1 memory array structure. It features a central horizontal bit line (BL) and two diagonal word lines (WL). The array is divided into two vertical sections, MA0 and MA1, indicated by brackets on the left. Each section contains two vertical columns of components. In the MA1 section, a downward-pointing arrow indicates current flow from the top WL line, through a variable resistor (VR), a memory cell (MC), and a sense diode (SD) to the BL. In the MA0 section, an upward-pointing arrow indicates current flow from the BL, through a sense diode (SD), a memory cell (MC), and a variable resistor (VR) to the bottom WL line. The components are labeled WL, VR, MC, SD, and BL.

FIG. 22



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FIG. 23

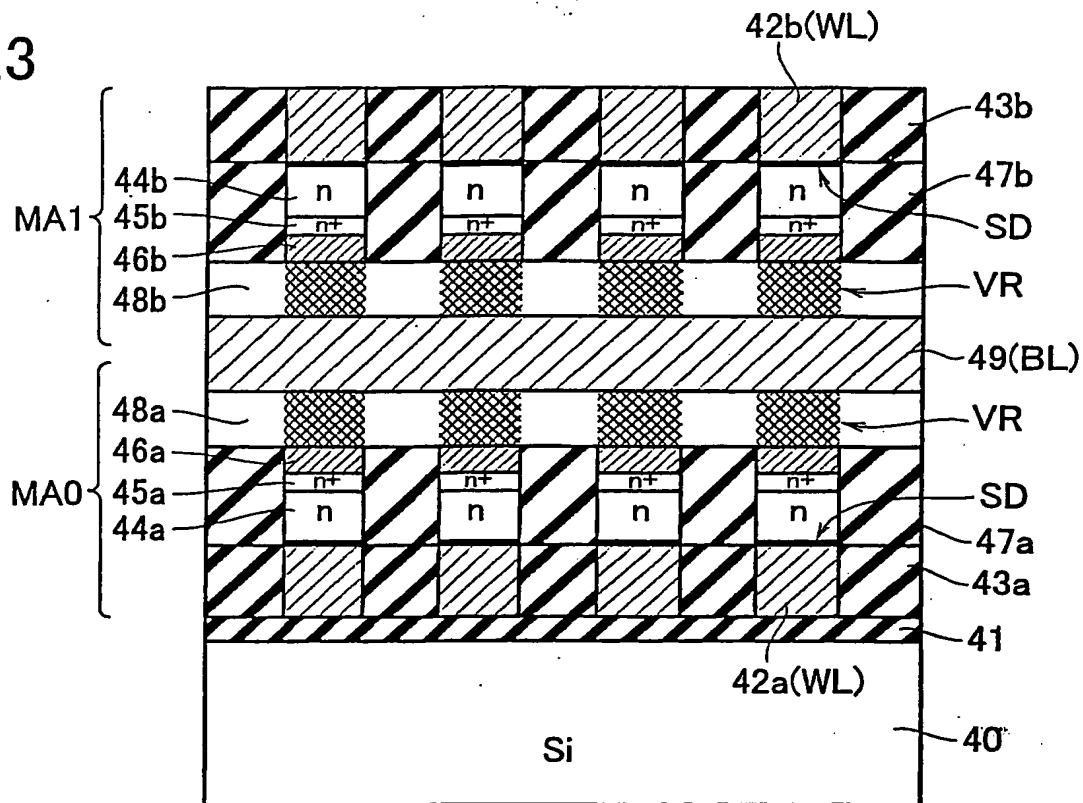


FIG. 24

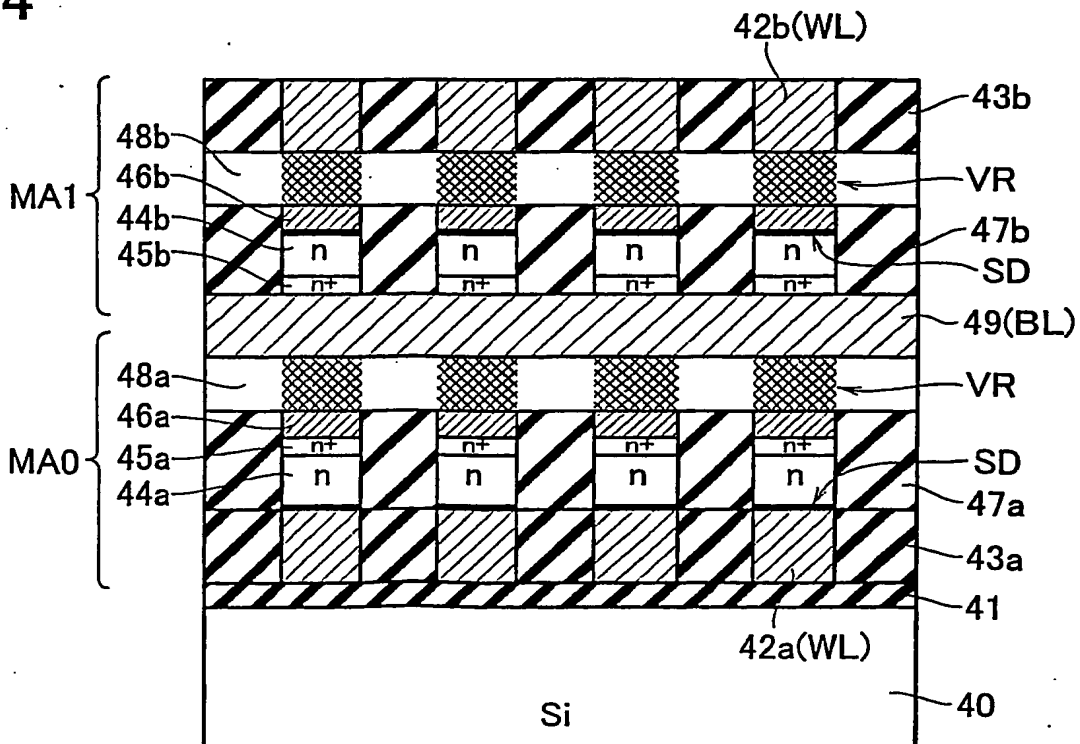


FIG. 25

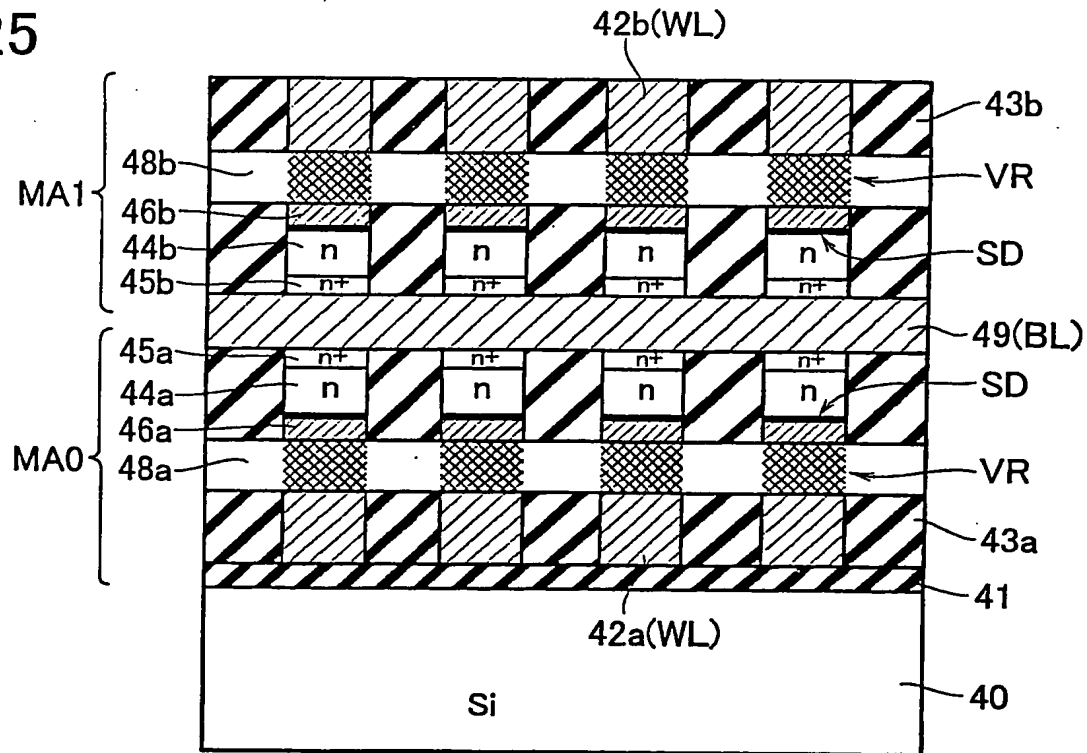
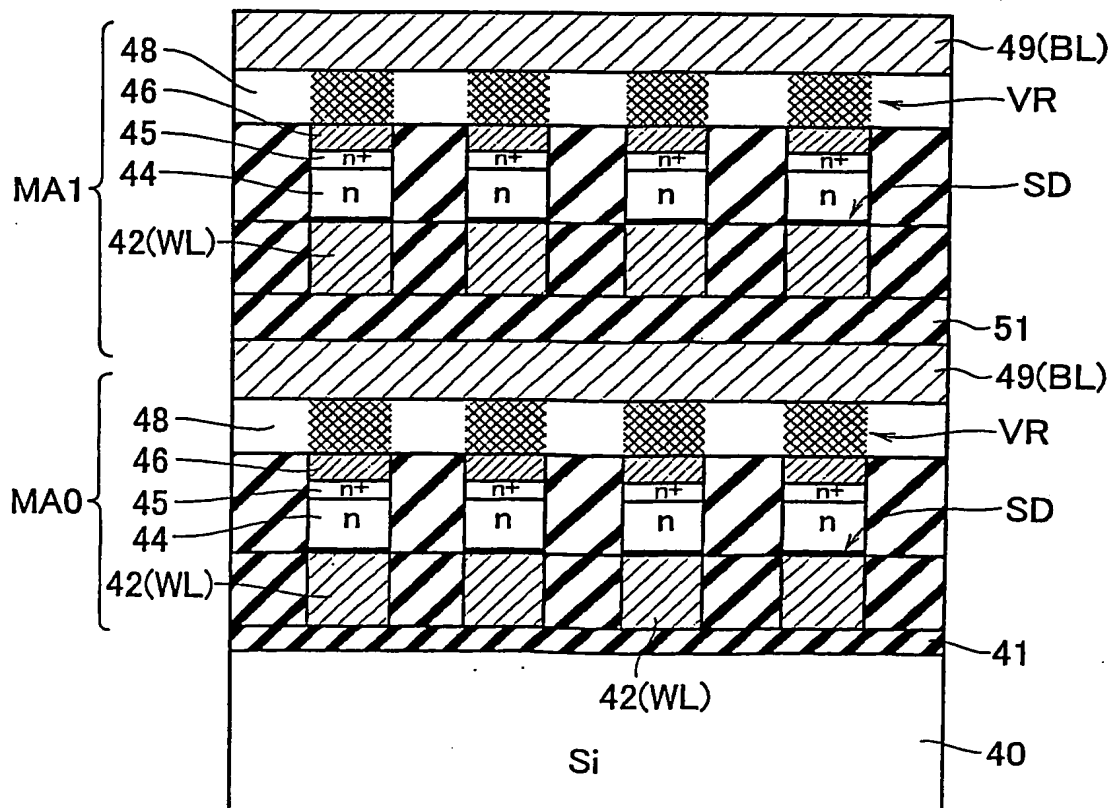


FIG. 26



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FIG. 27

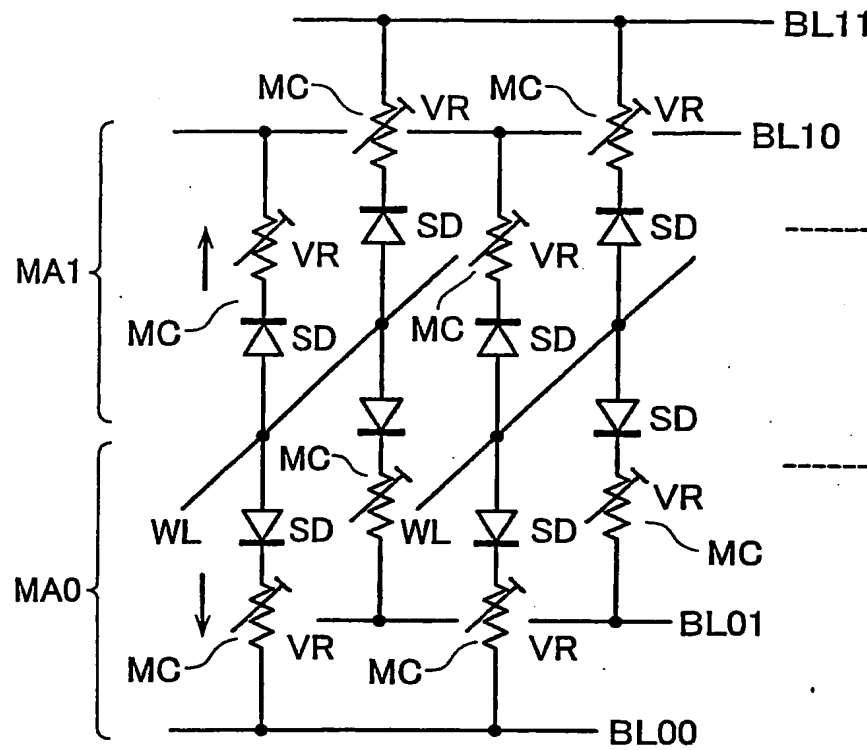
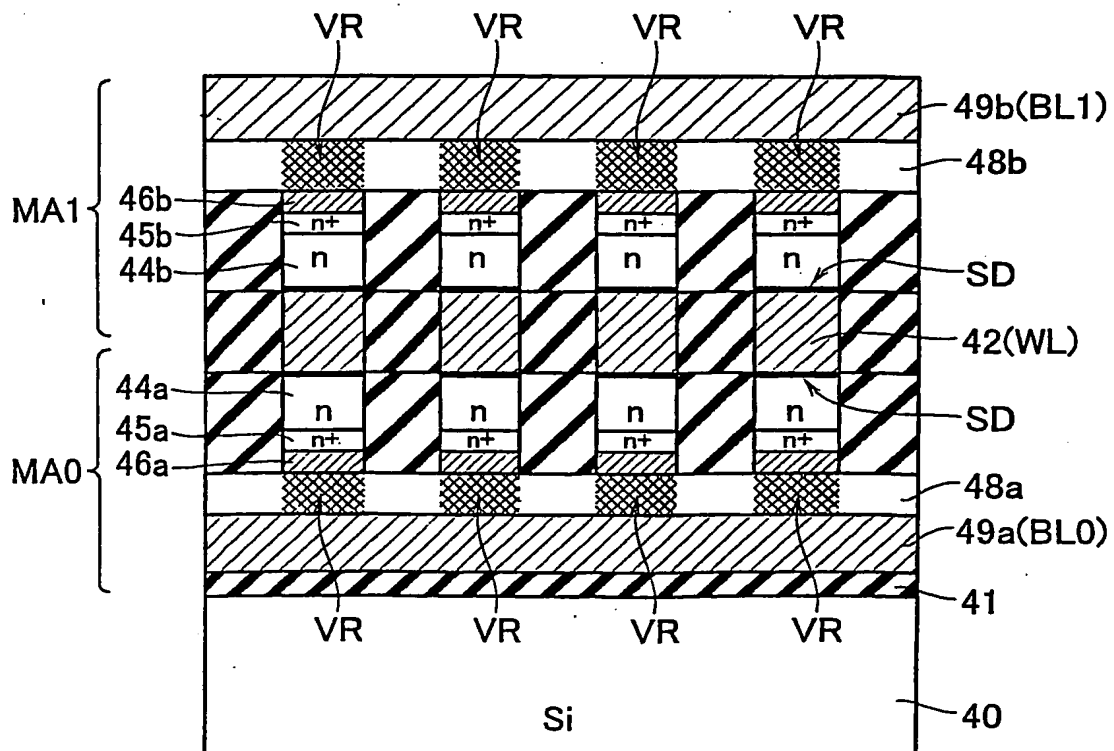
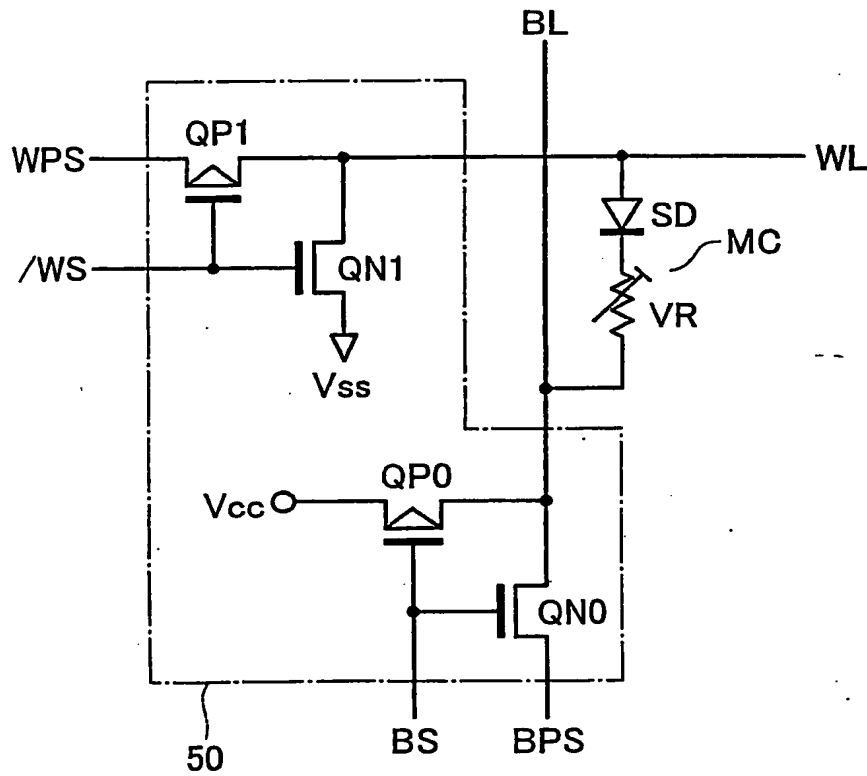


FIG. 28



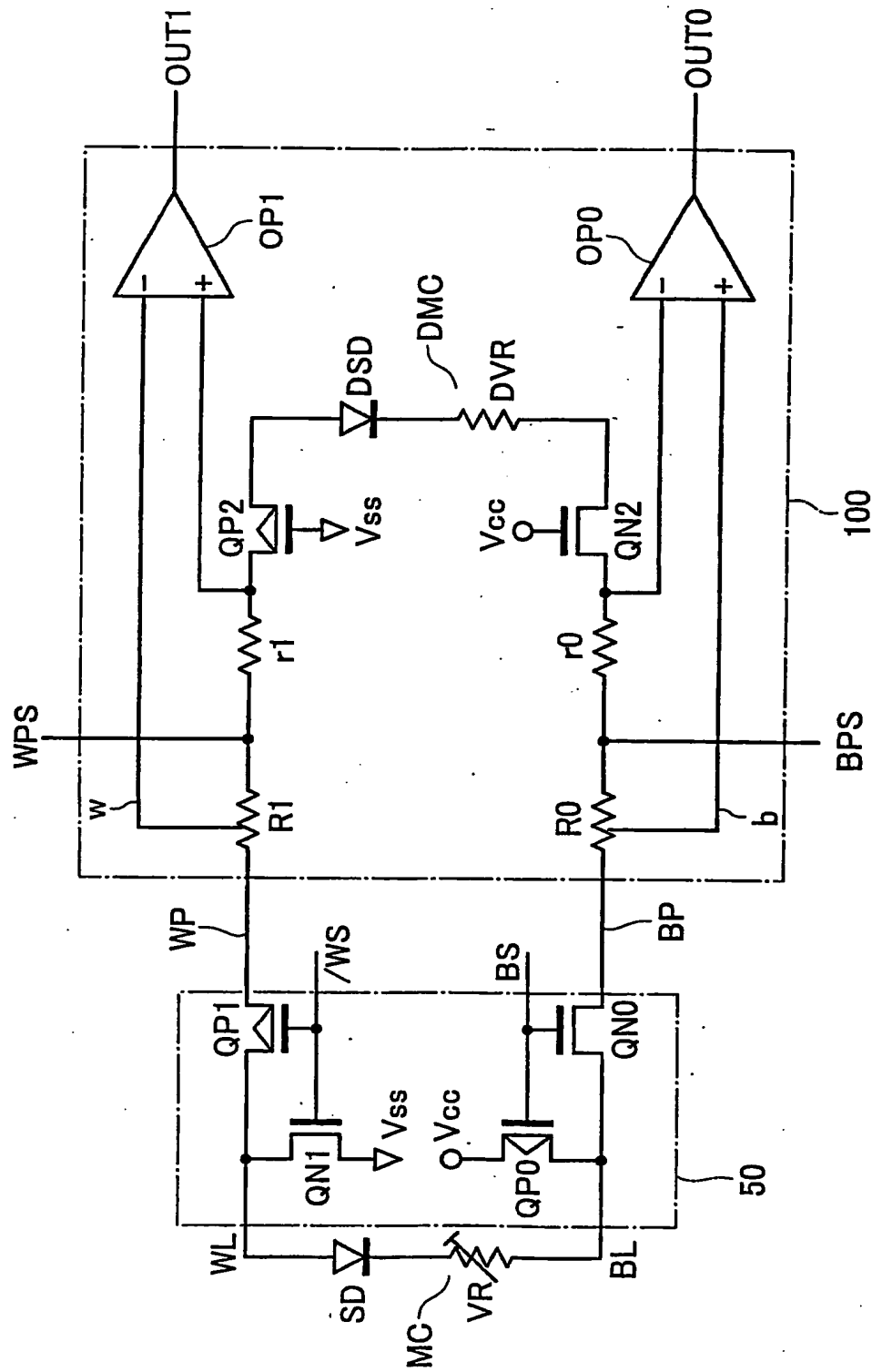
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FIG. 29



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FIG. 30





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FIG. 31

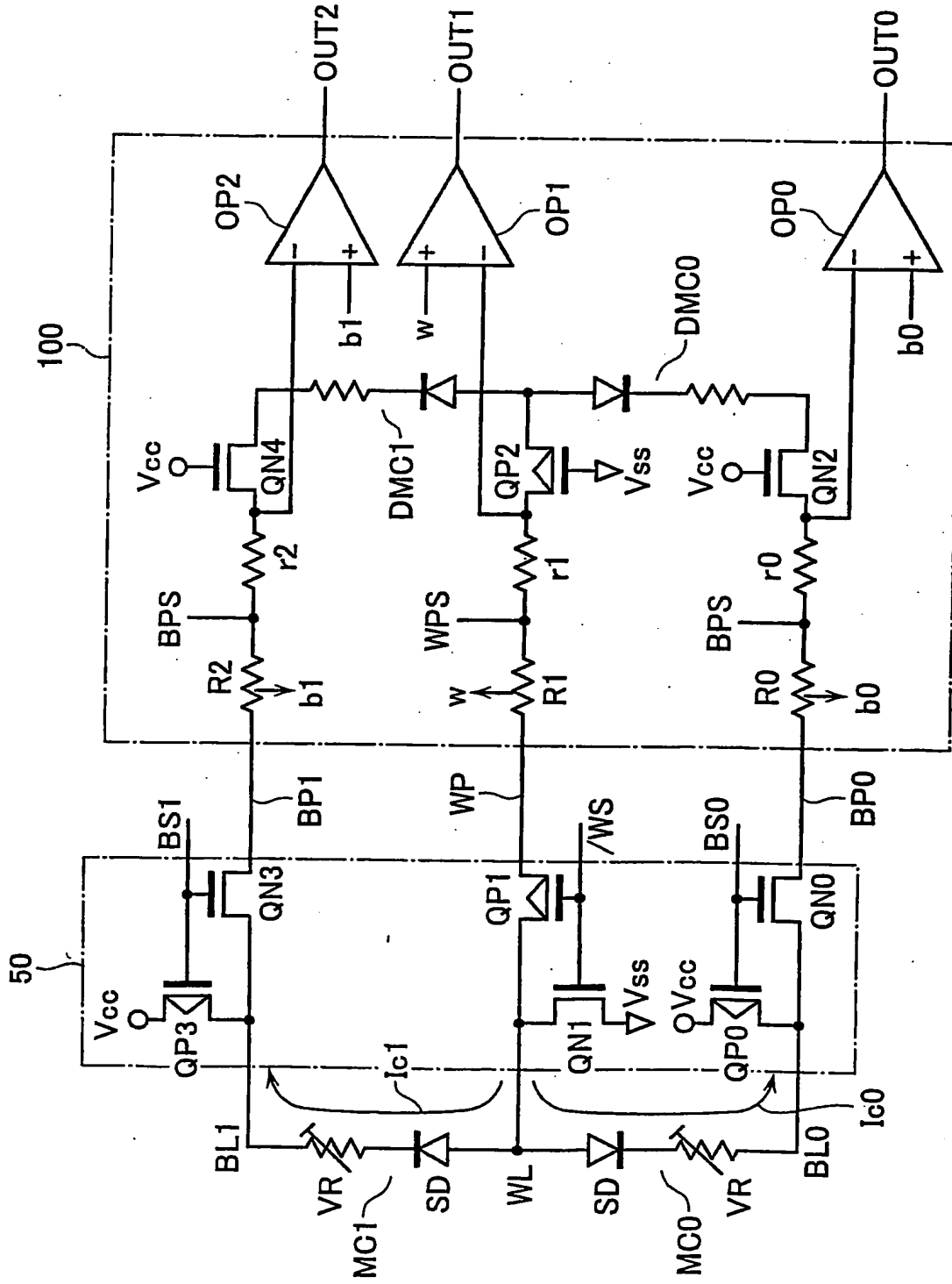


FIG. 32

	0	1
OUT0	L	H
OUT1	L	H

FIG. 33

	00	01	10	11
OUT2	—	L	—	H
OUT1	L	H	H	H
OUT0	—	—	L	H

FIG. 34

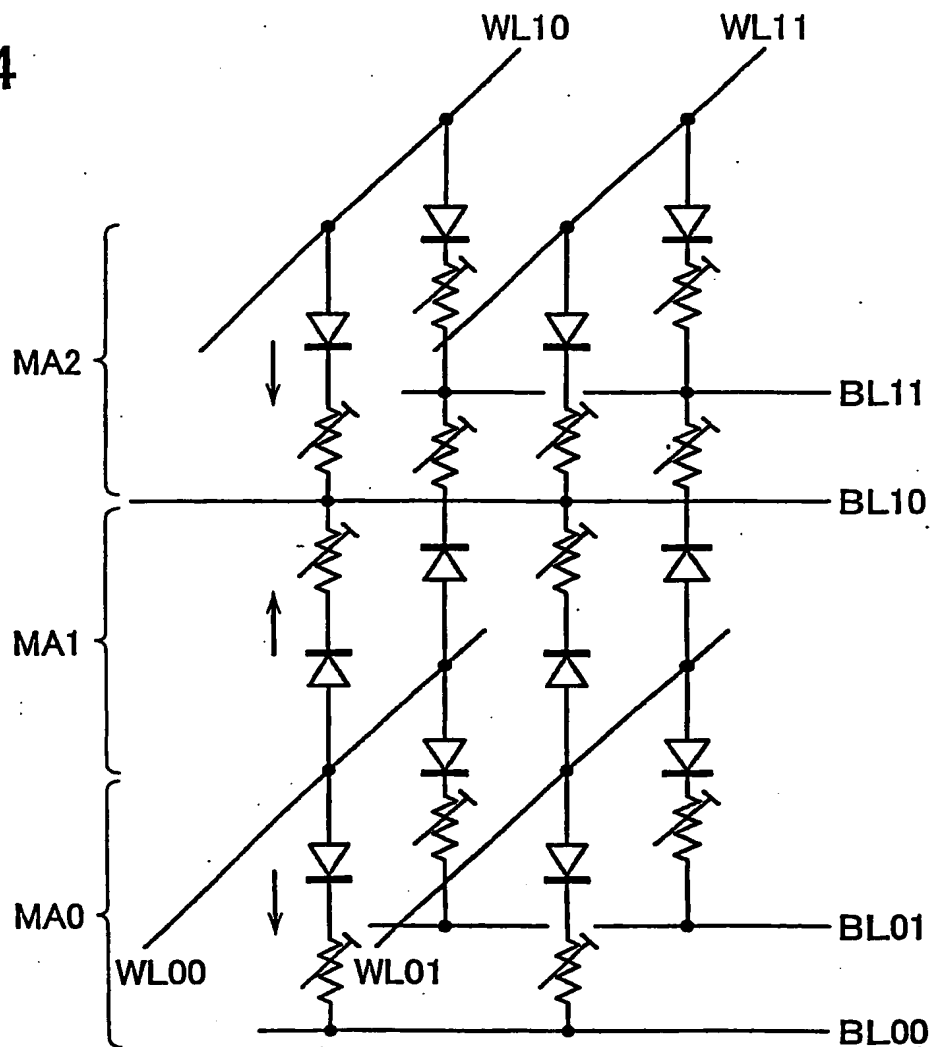
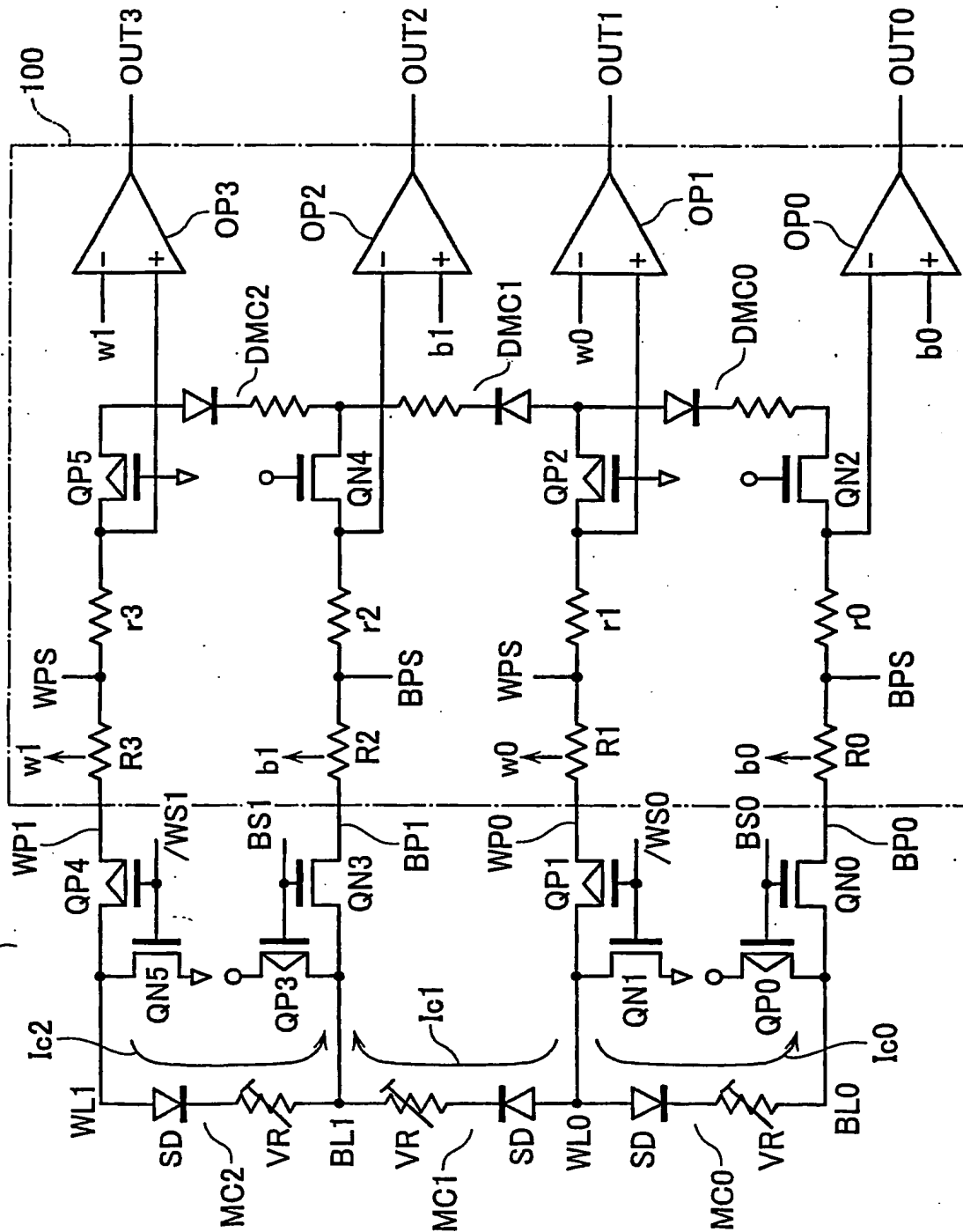


FIG. 36

	000	001	010	011	100	101	110	111
OUT3	—	—	L	L	—	H	H	H
OUT2	L	L	—	H	H	H	—	H
OUT1	L	H	H	—	L	H	H	H
OUT0	—	—	L	H	—	H	L	H

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FIG. 37

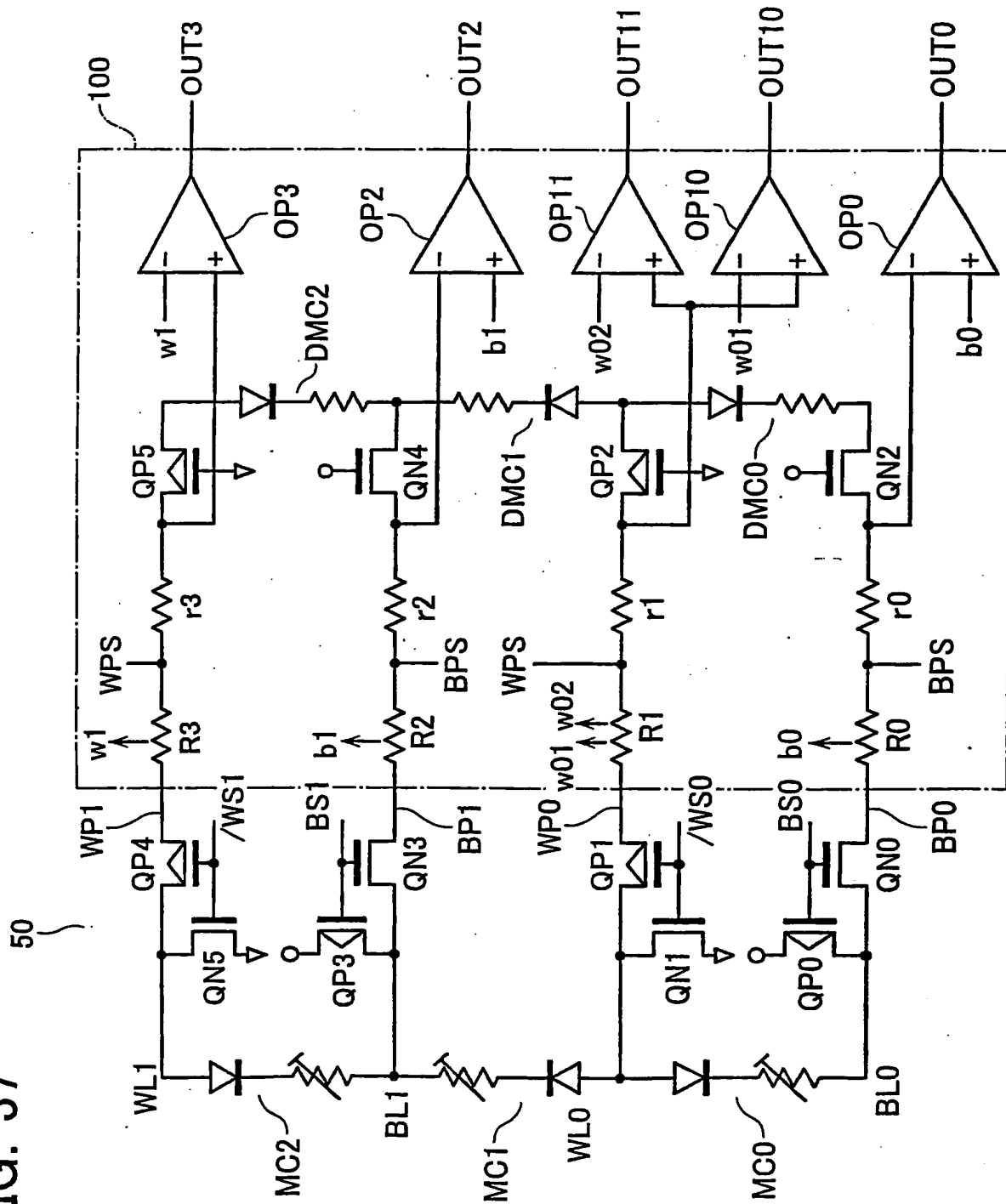


FIG. 38

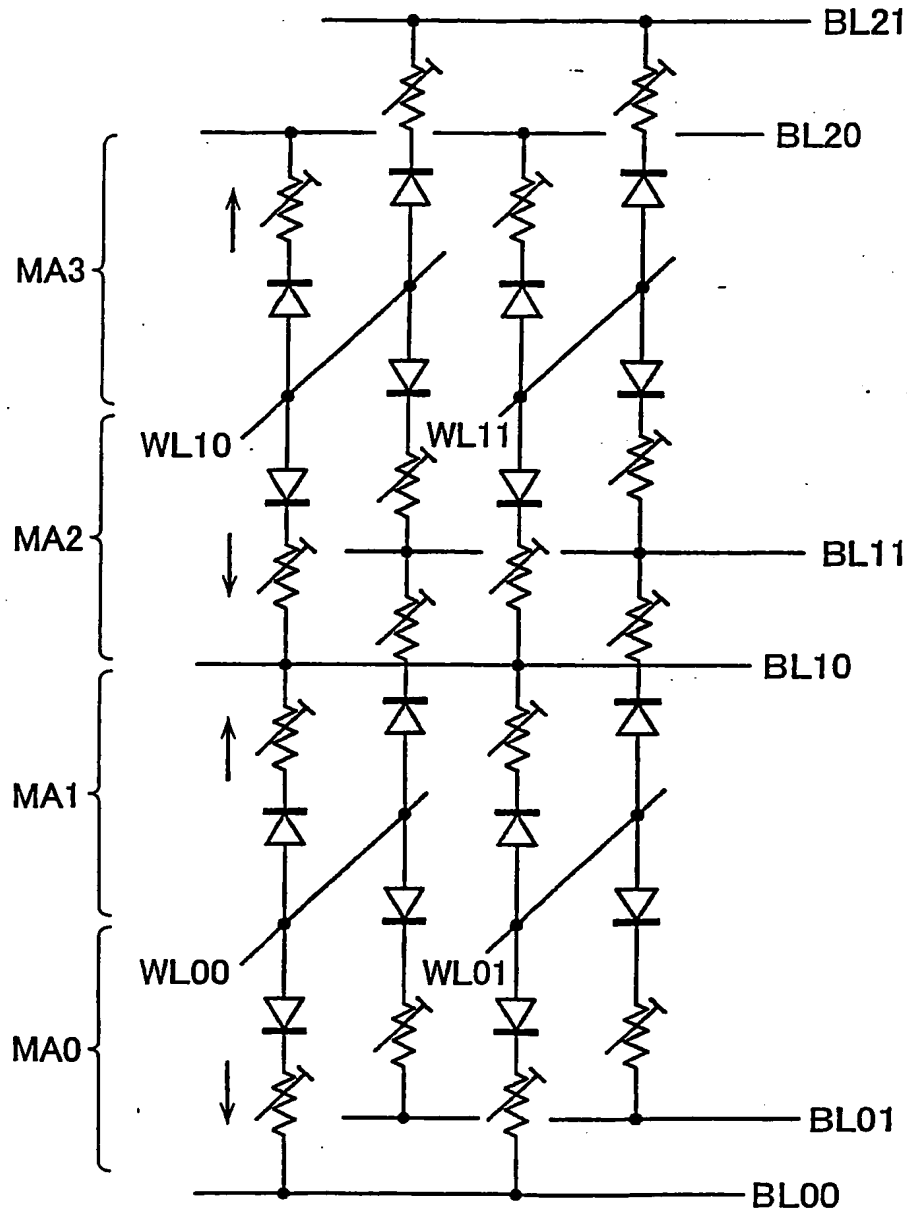
	000	001	010	011	100	101	110	111
OUT3	L	L	L	L	H	H	H	H
OUT10	L	H	H	—	L	H	H	—
OUT11	—	—	—	H	—	—	—	H
OUT0	—	H	L	—	—	H	L	—

FIG. 39

	00	01	10	11
OUT10	L	H	H	H
OUT11	—	L	L	H
OUT0	—	L	H	—

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FIG. 40



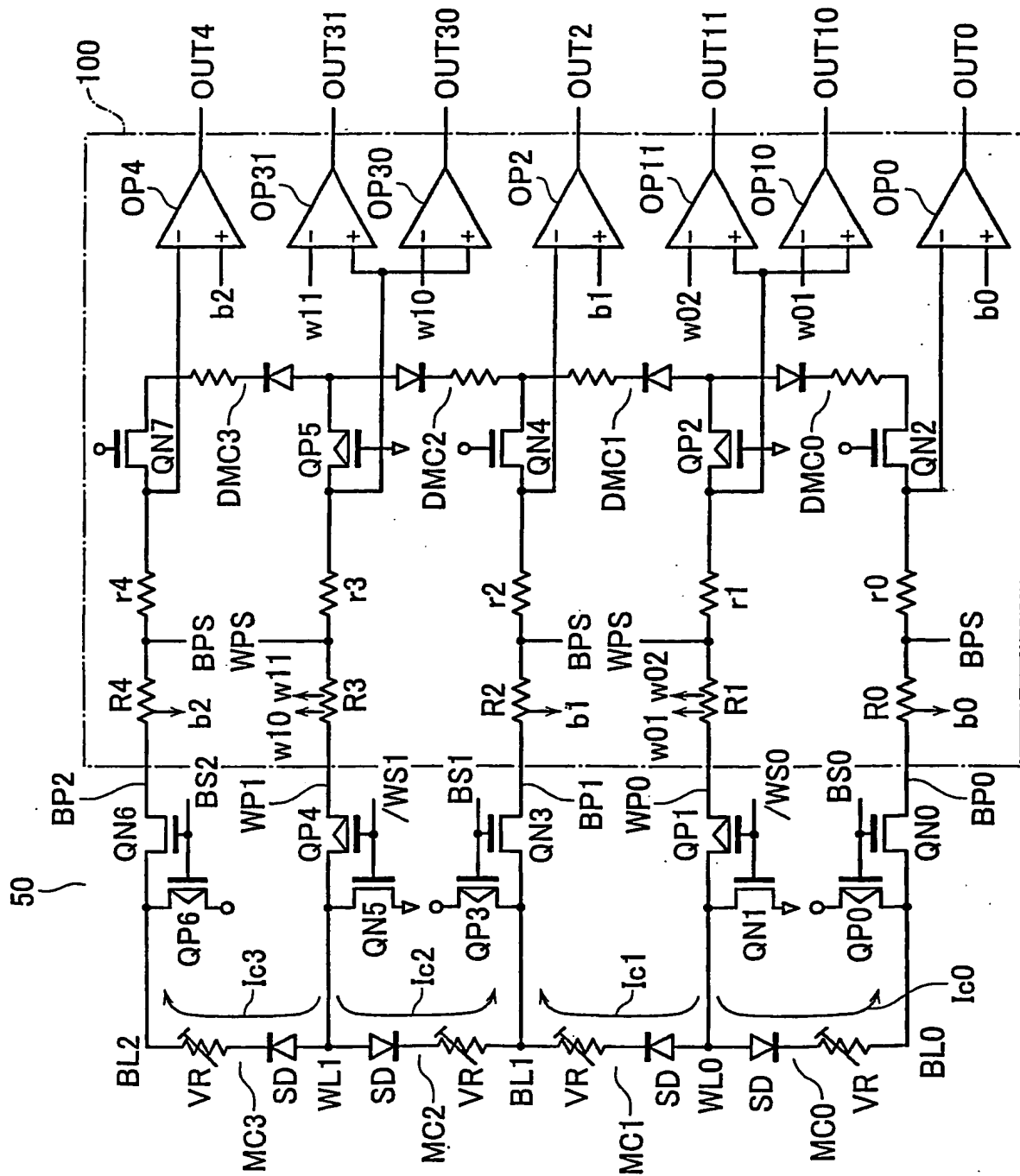
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FIG. 41

	0000	0001	0010	0011	0100	0101	0110	0111
OUT4	—	—	—	—	L	L	L	L
OUT3	L	L	L	L	—	H	H	H
OUT2	—	L	H	H	H	H	—	H
OUT1	L	H	—	H	L	H	H	H
OUT0	—	—	L	H	—	H	L	H
	1000	1001	1010	1011	1100	1101	1110	1111
OUT4	—	—	H	H	H	H	H	H
OUT3	H	H	H	H	—	H	H	H
OUT2	L	L	H	H	H	H	H	H
OUT1	L	H	H	H	L	H	H	H
OUT0	—	—	L	H	—	H	L	H



FIG. 42



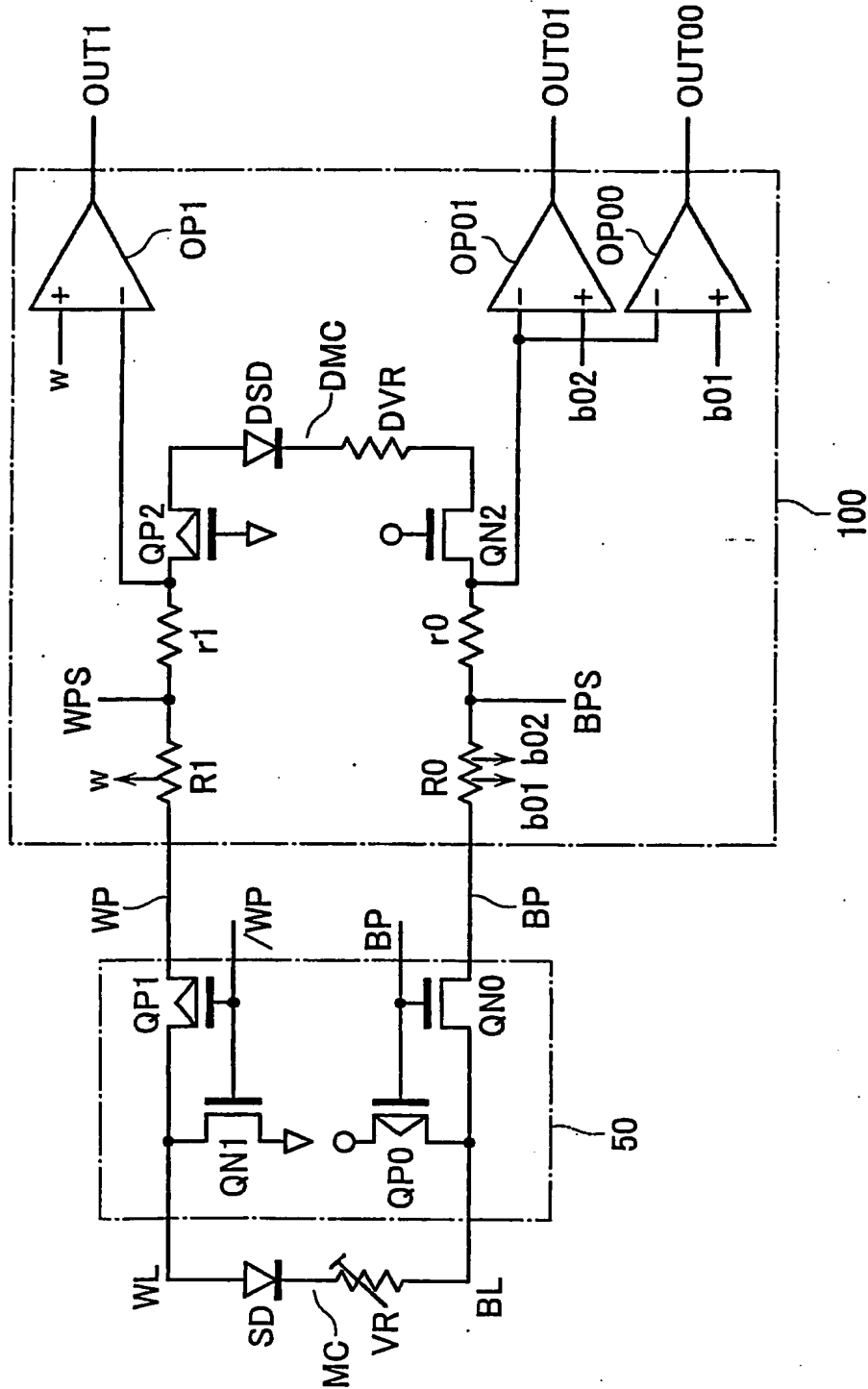
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FIG. 43

	0000	0001	0010	0011	0100	0101	0110	0111
OUT4	-	-	-	-	L	L	L	L
OUT30	L	L	L	L	H	H	H	H
OUT31	-	-	-	-	-	-	-	-
OUT10	L	H	H	-	L	H	H	-
OUT11	-	L	-	H	-	L	-	H
OUT0	-	H	L	-	-	H	L	-
	1000	1001	1010	1011	1100	1101	0110	1111
OUT4	H	H	H	H	-	-	-	-
OUT30	H	H	H	H	-	-	-	-
OUT31	L	L	L	L	H	H	H	H
OUT10	L	H	H	-	L	H	H	-
OUT11	-	L	-	H	-	L	-	H
OUT0	-	H	L	-	-	H	L	-

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FIG. 44



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FIG. 45

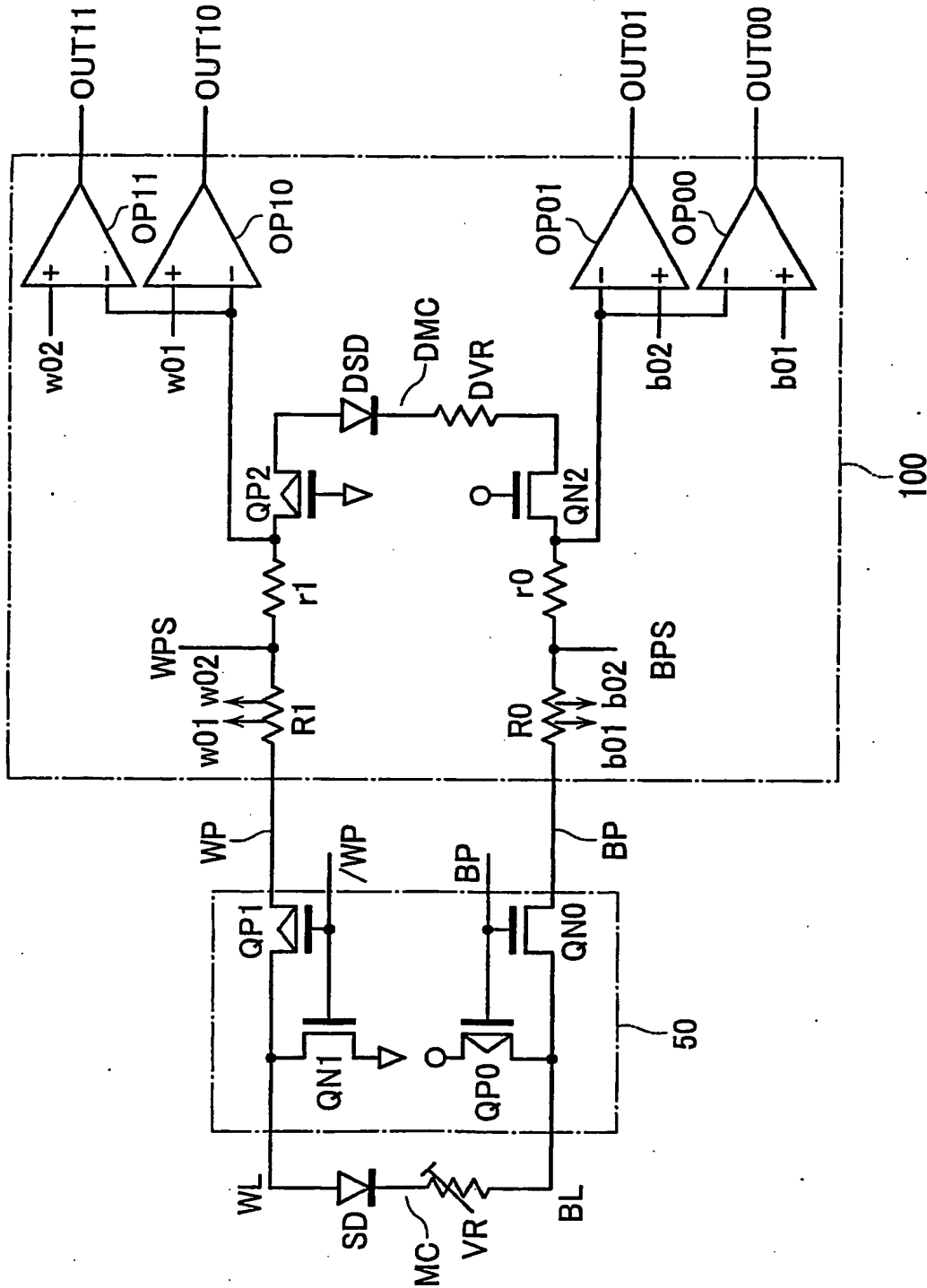


FIG. 46

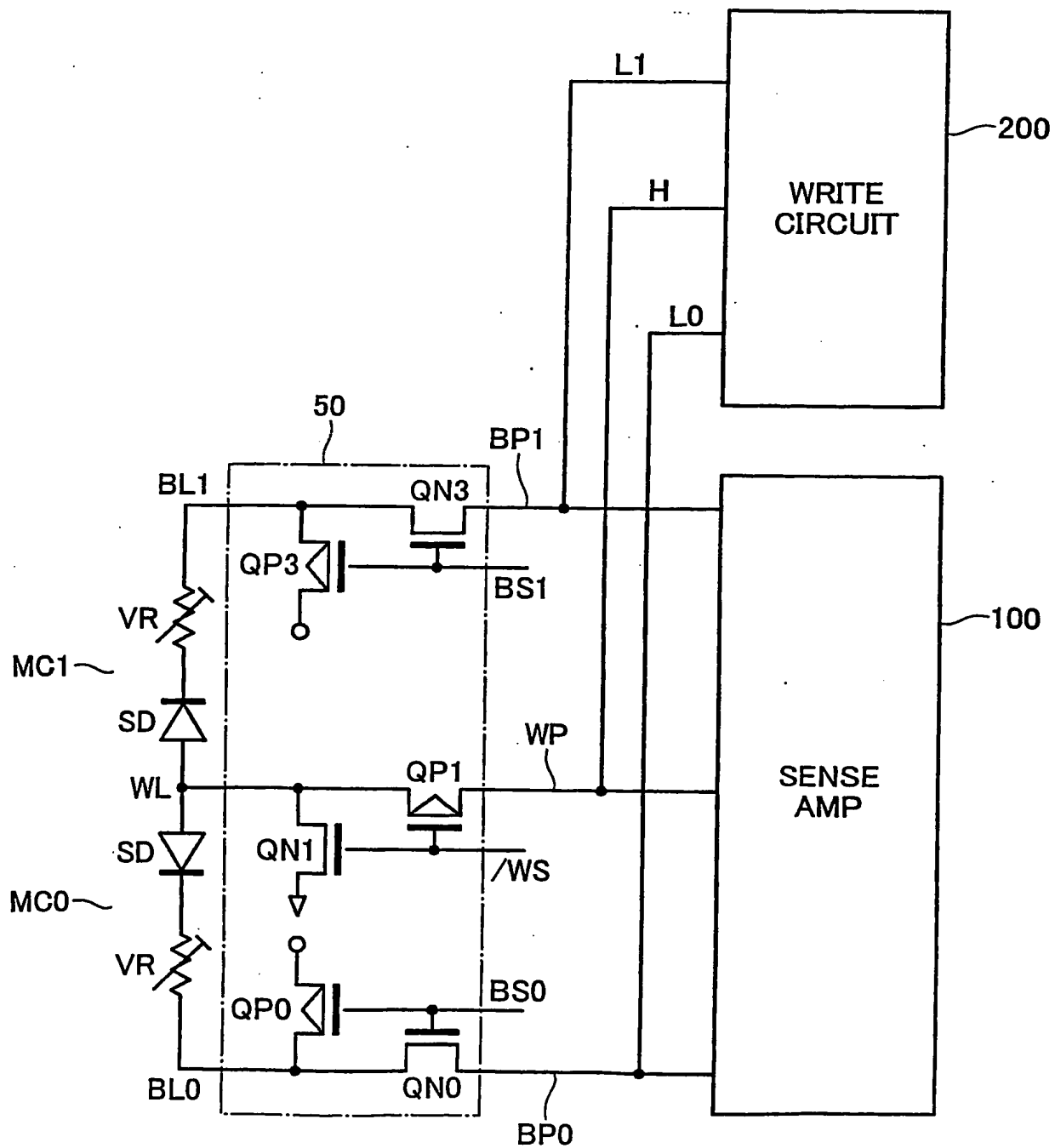


FIG. 47

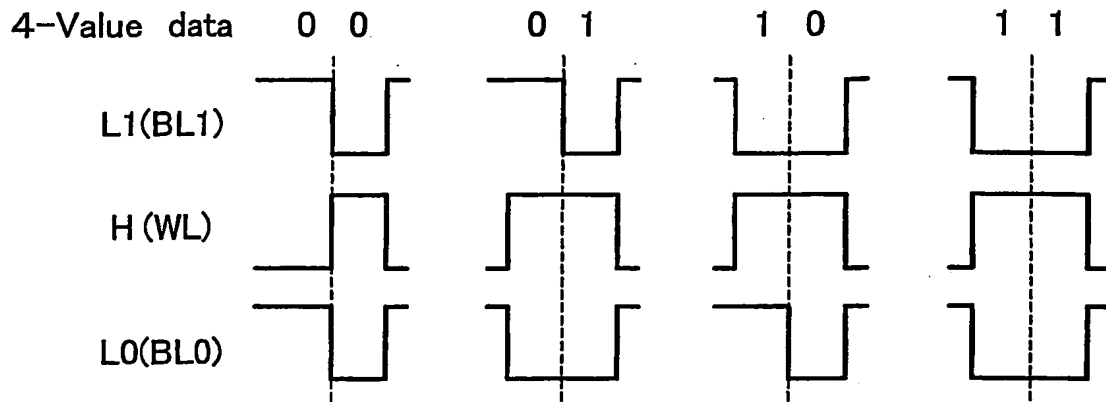


FIG. 48

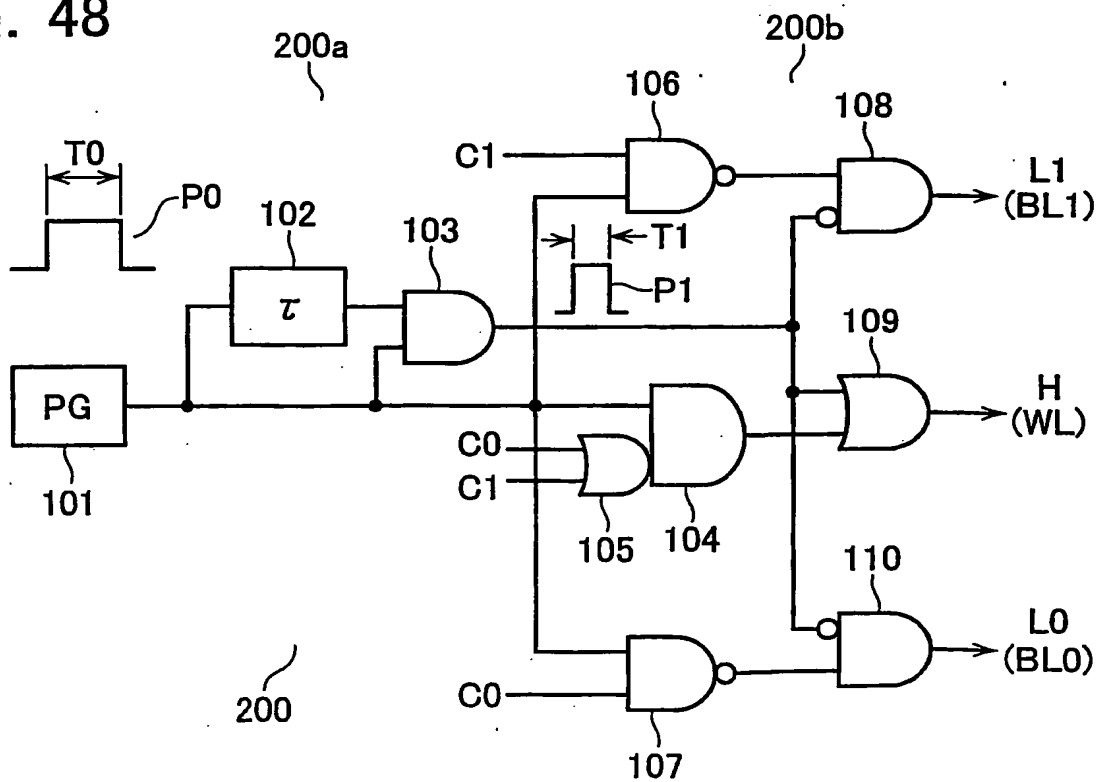


FIG. 49

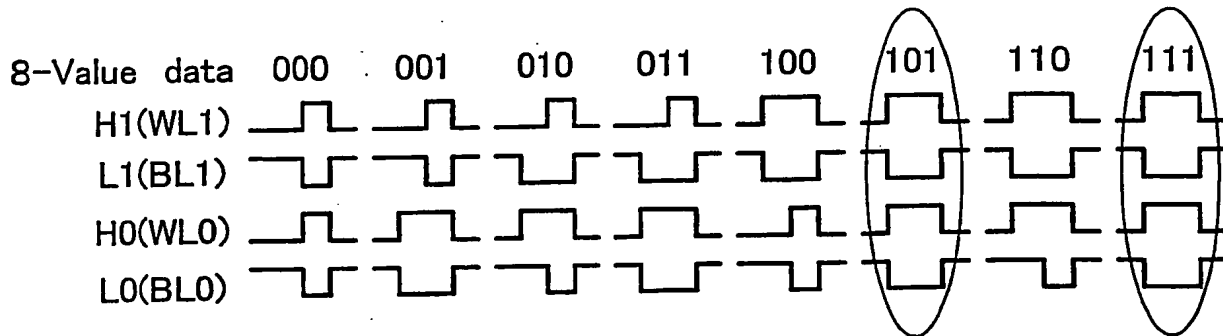
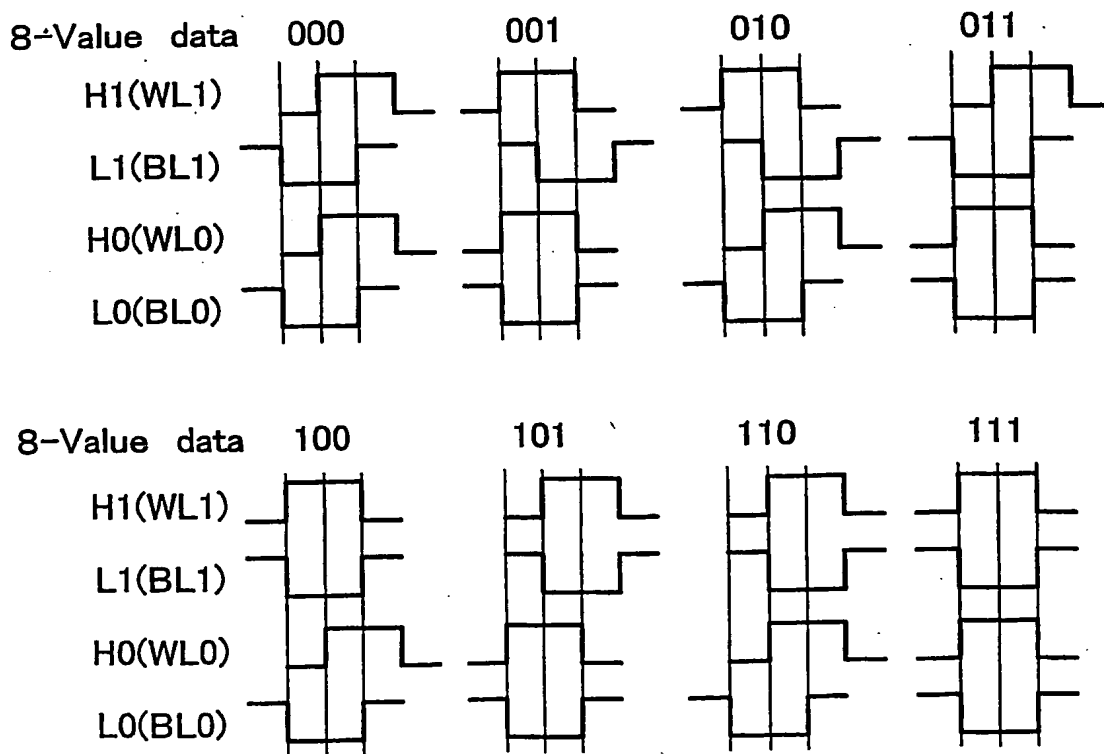


FIG. 50



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FIG. 51

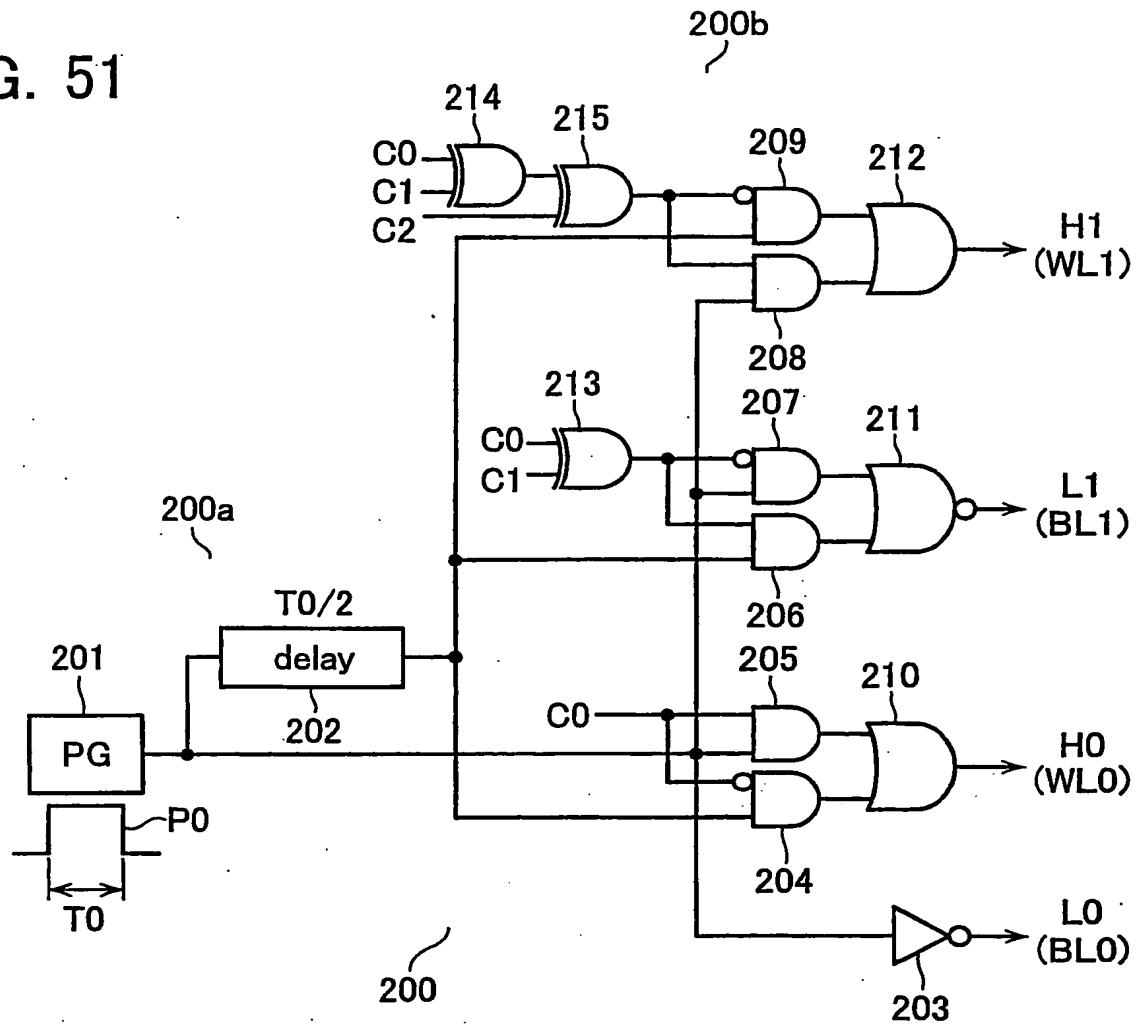


FIG. 52

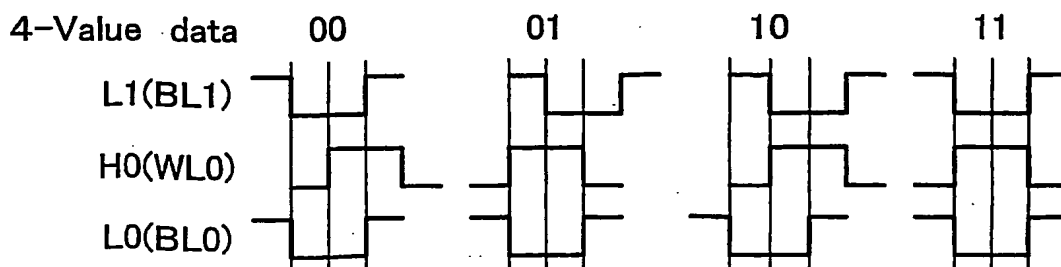




FIG. 53

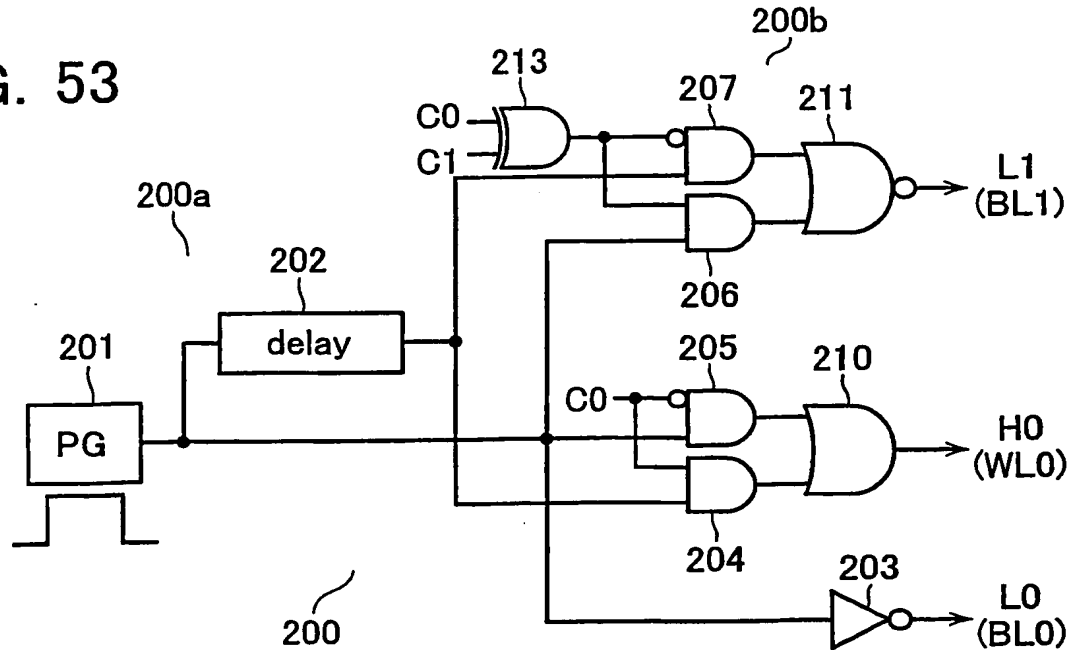


FIG. 55

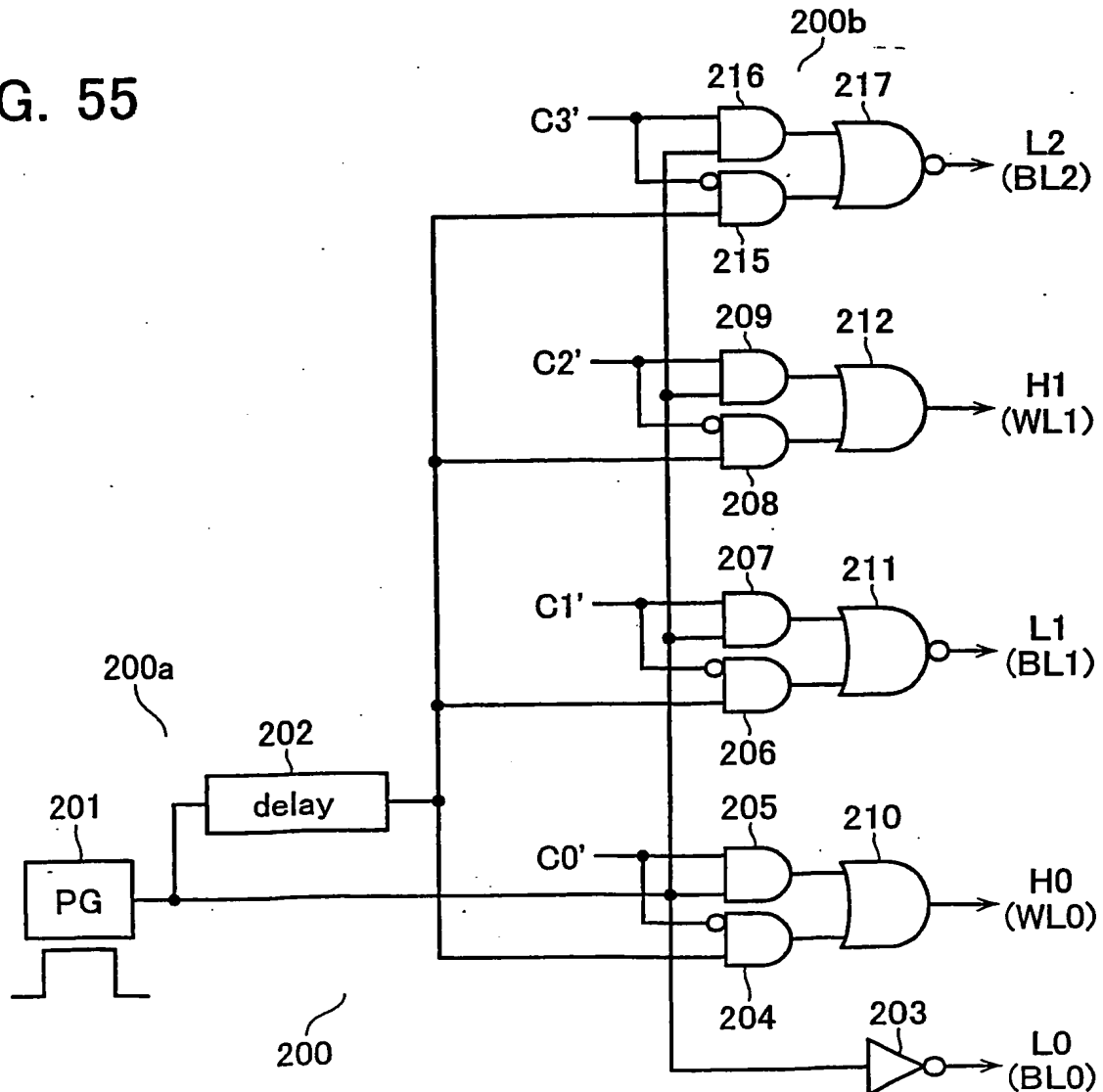


FIG. 54

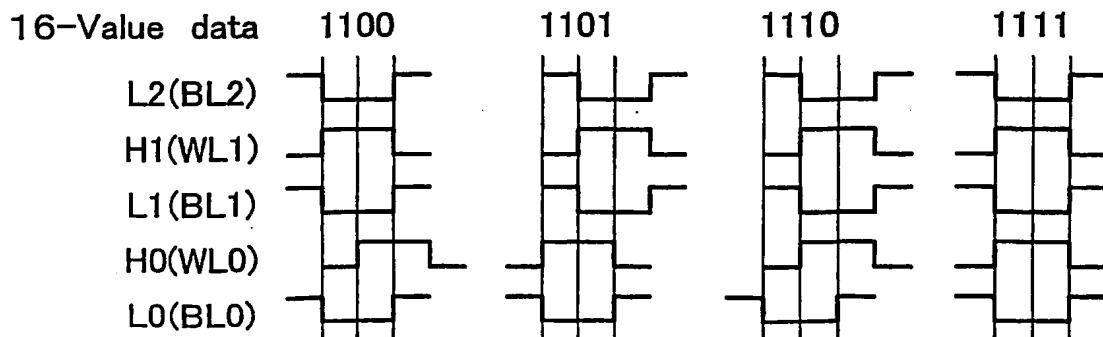
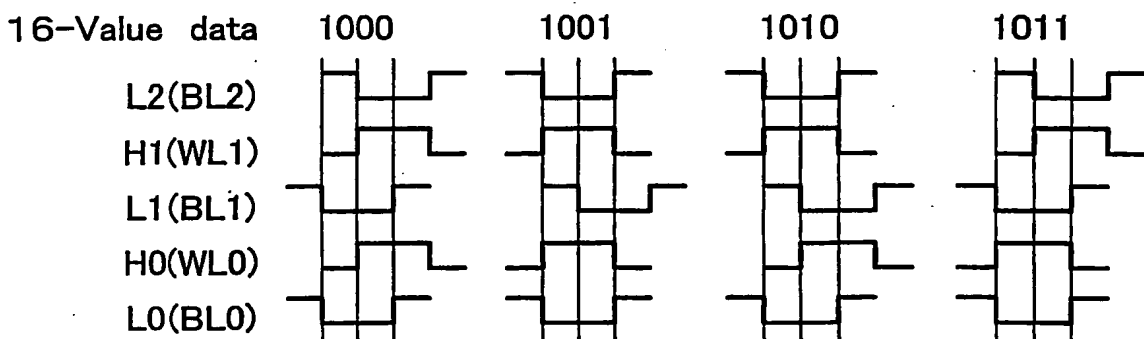
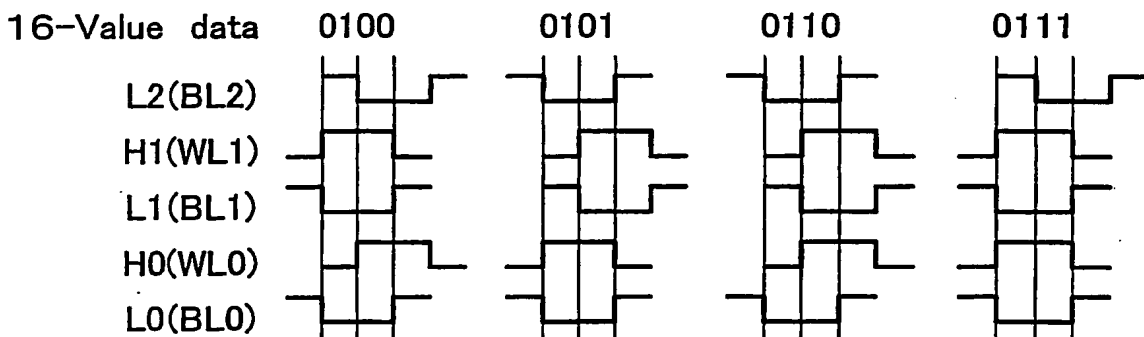
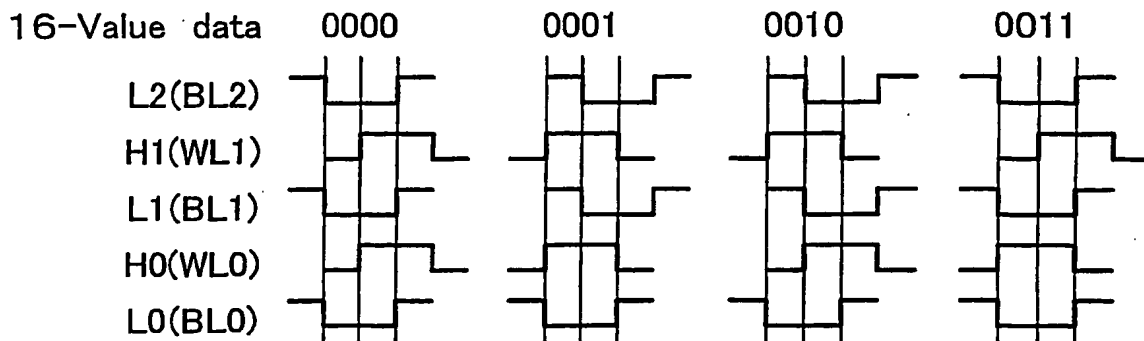


FIG. 56

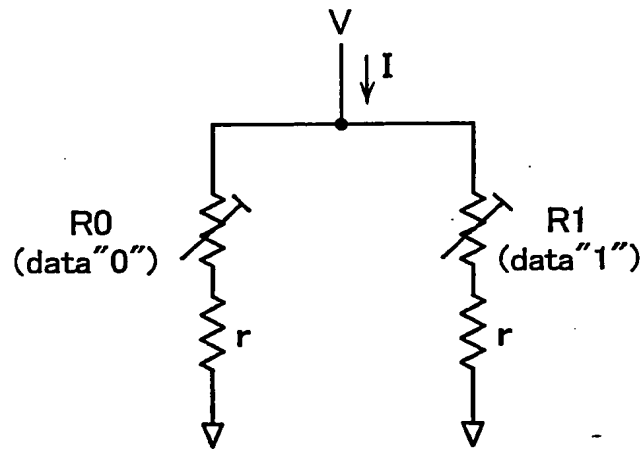
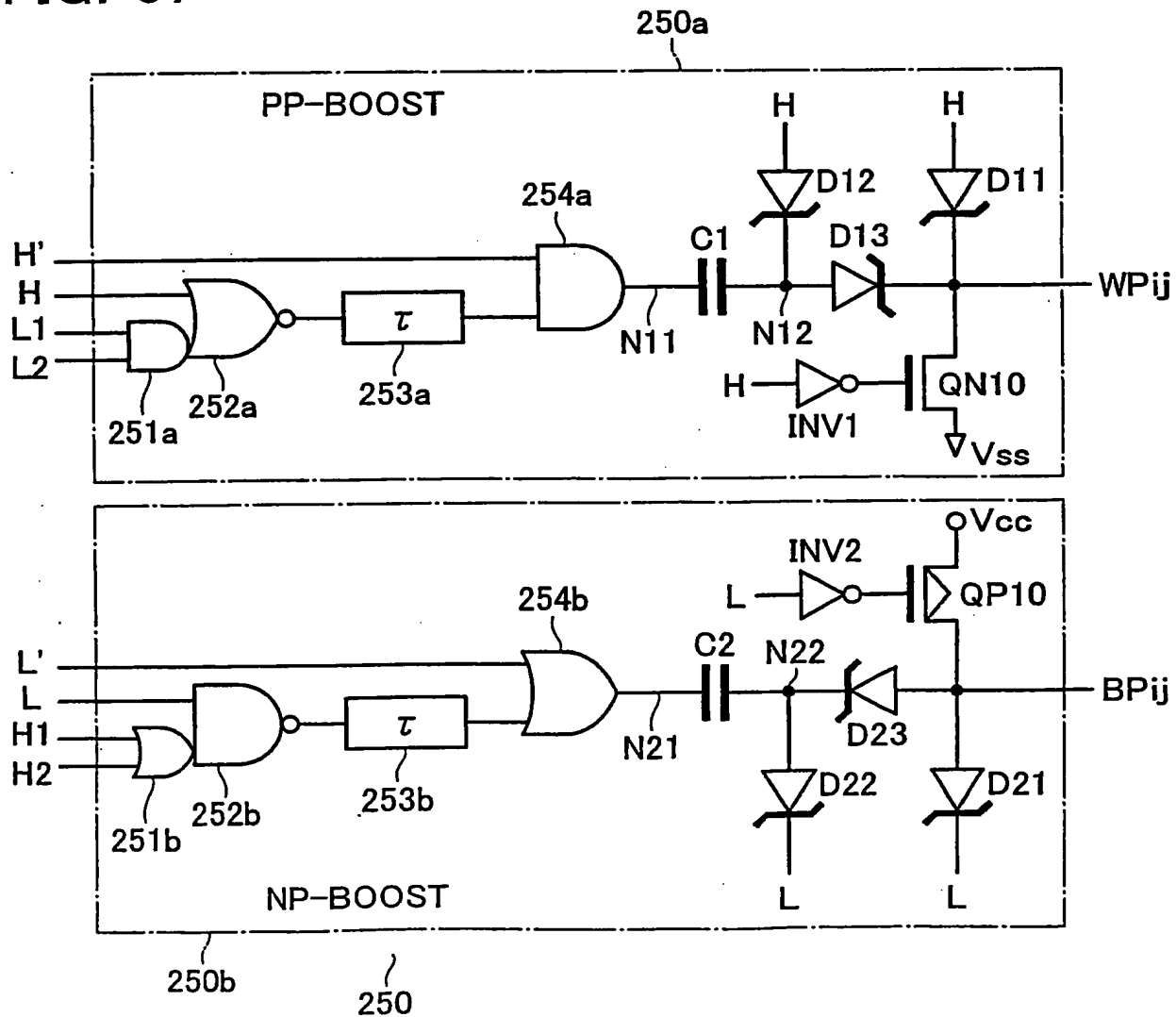


FIG. 57



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FIG. 58

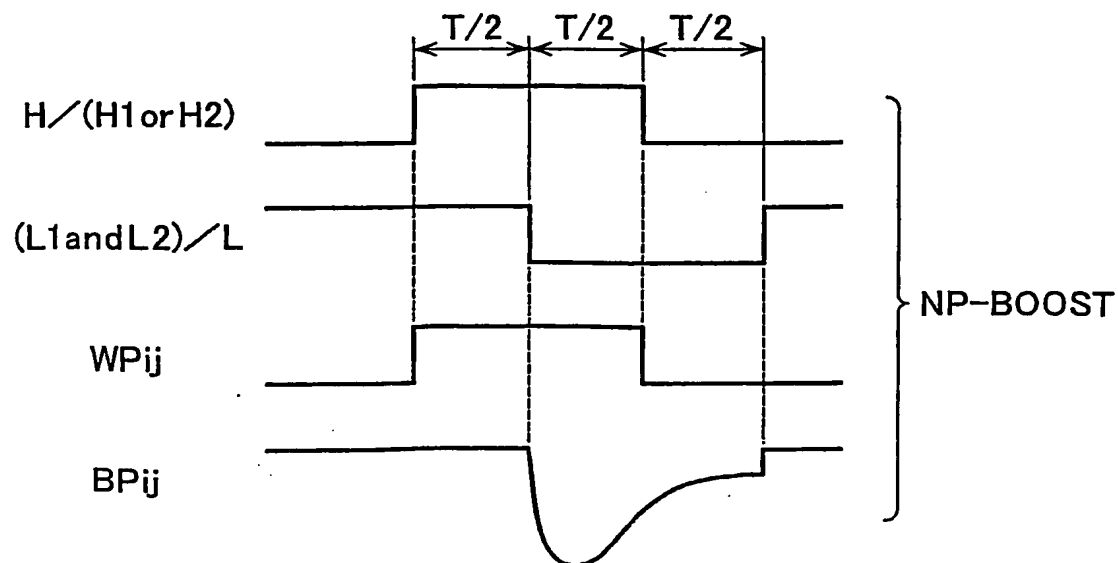
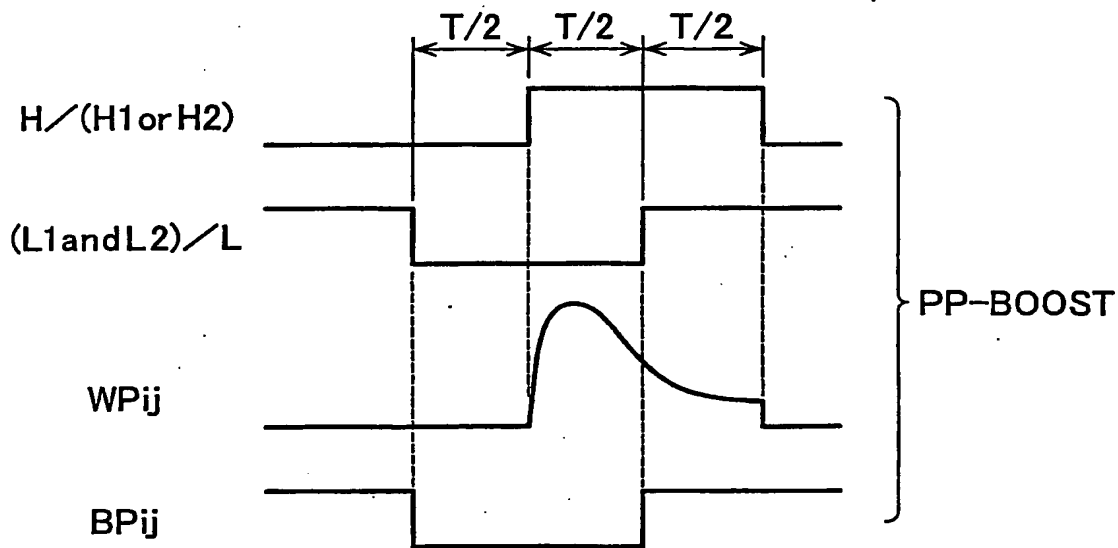
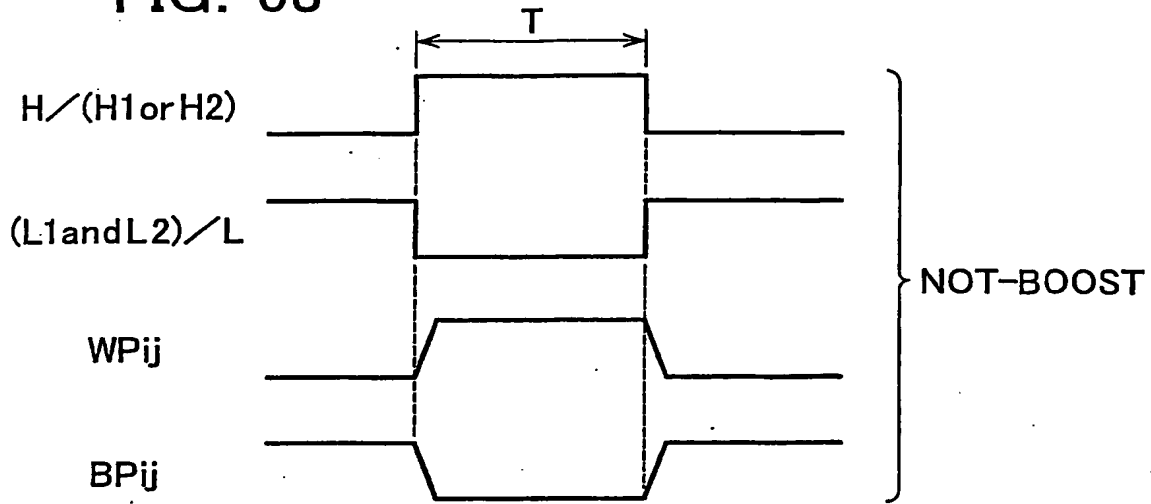
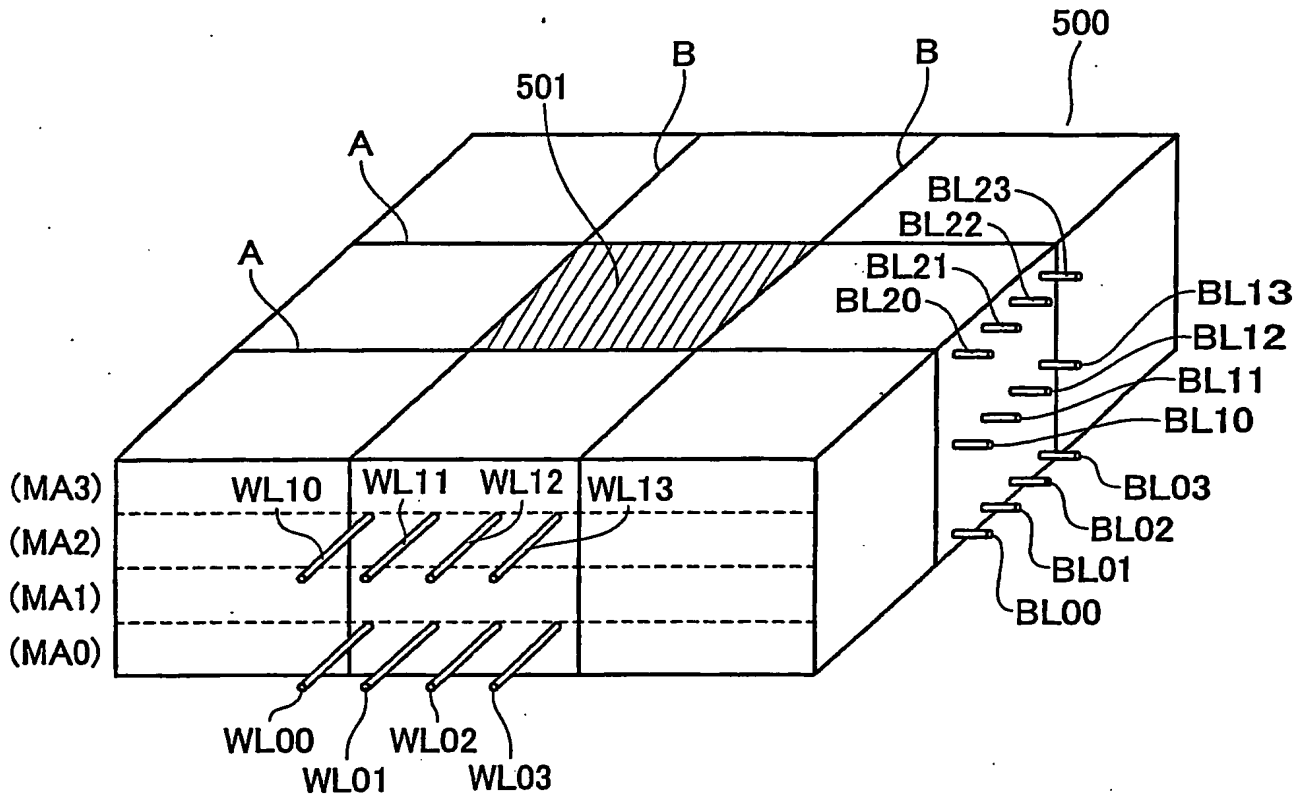


FIG. 59



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FIG. 60

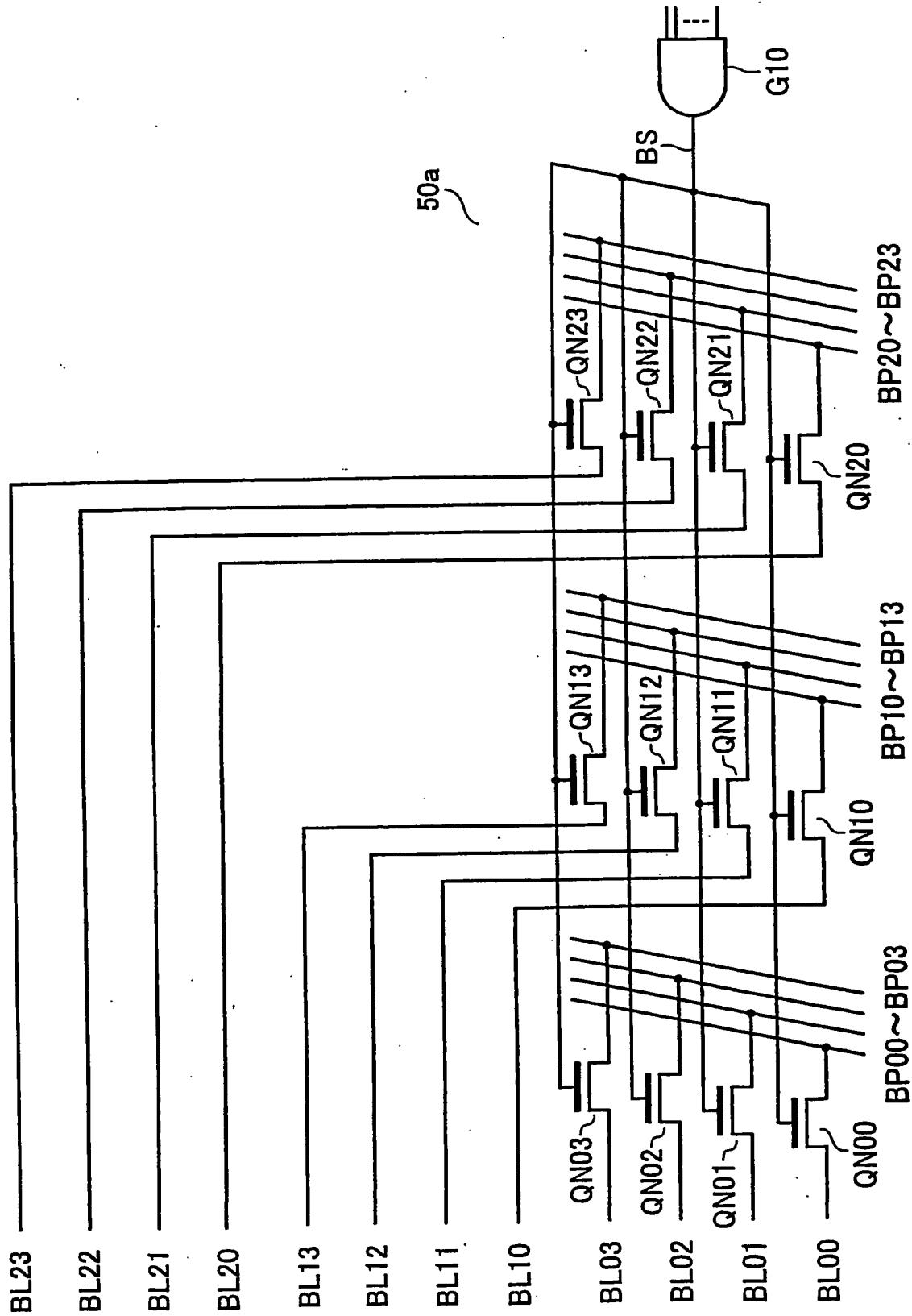
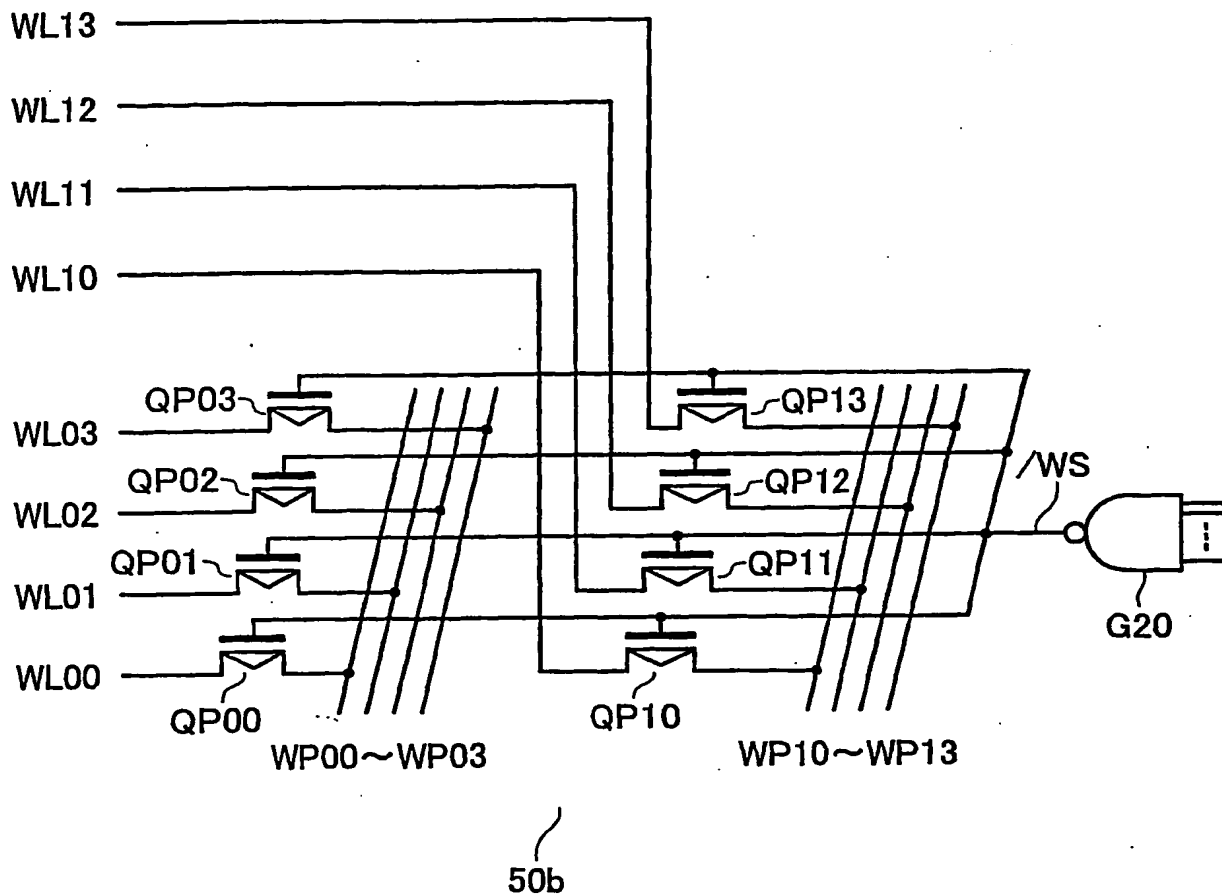


FIG. 61



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FIG. 62

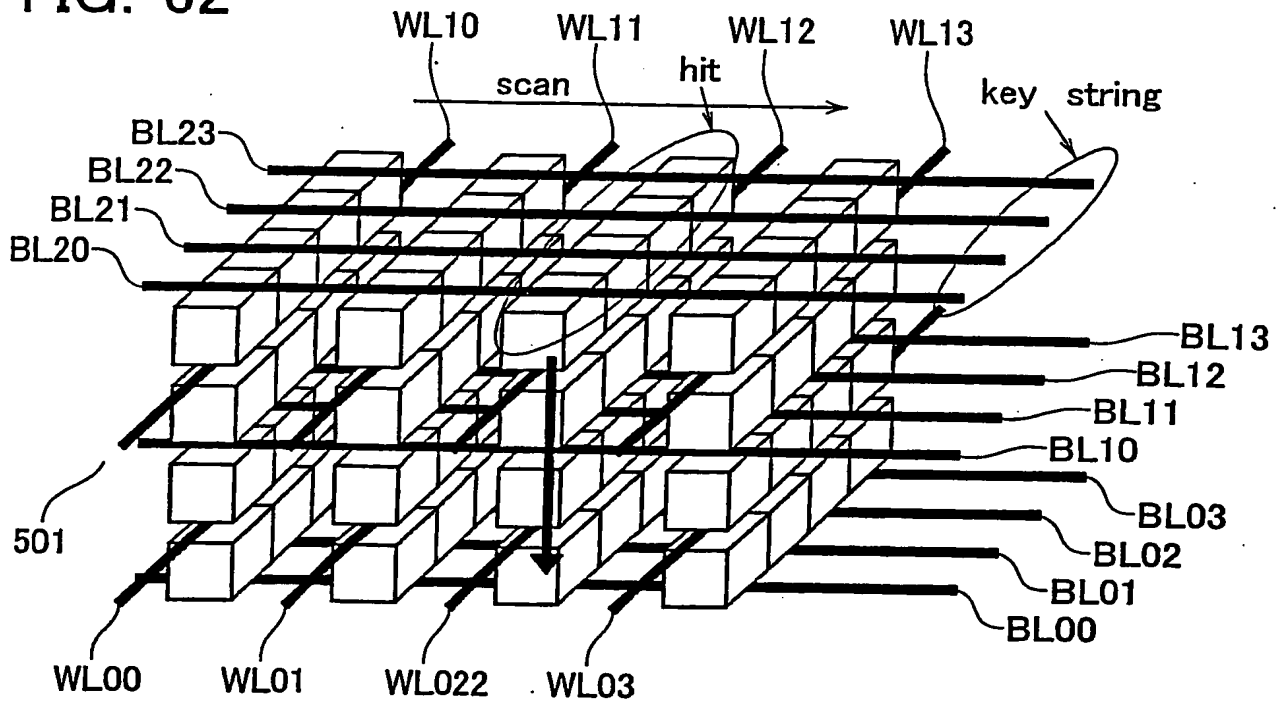
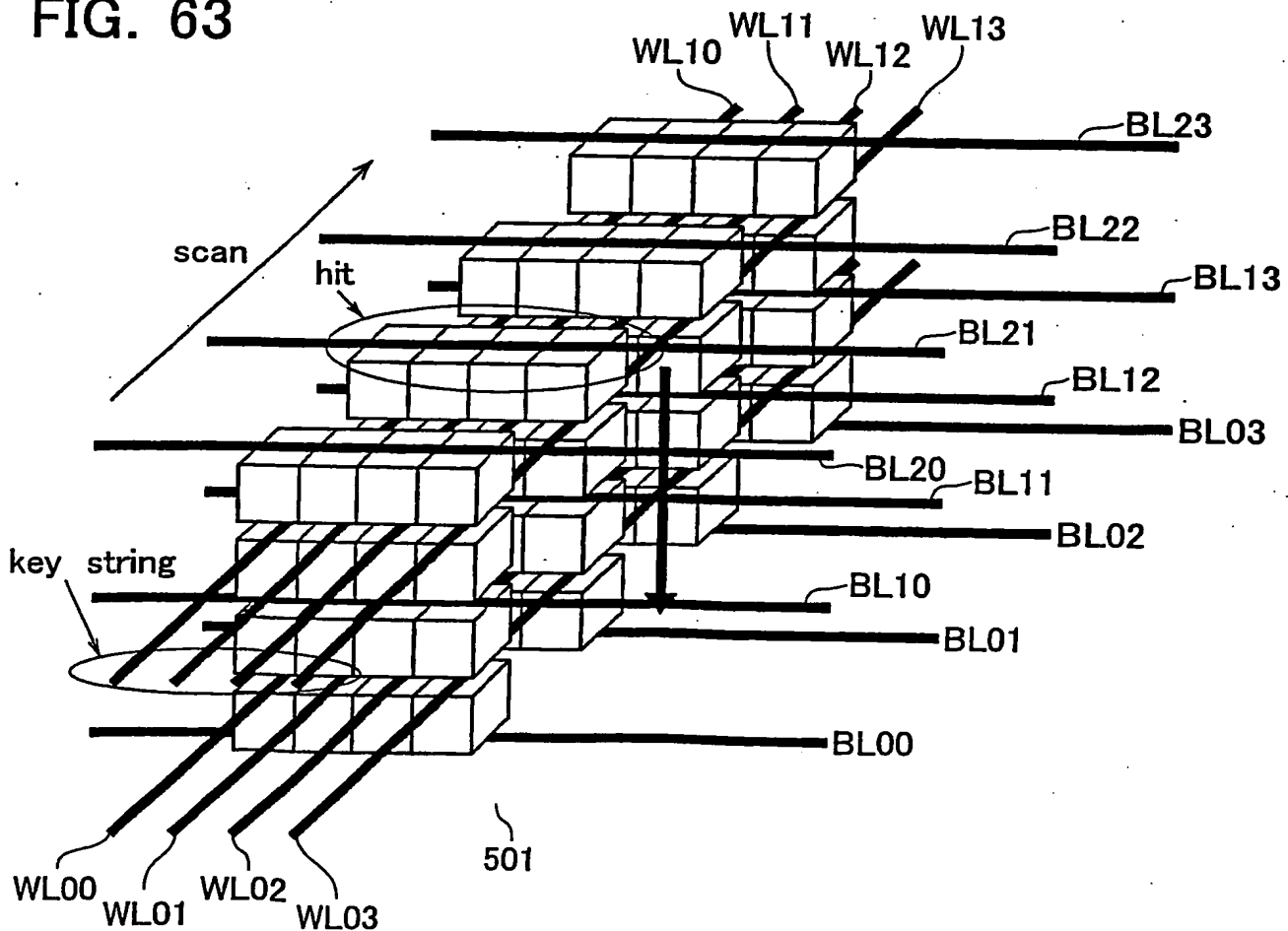


FIG. 63

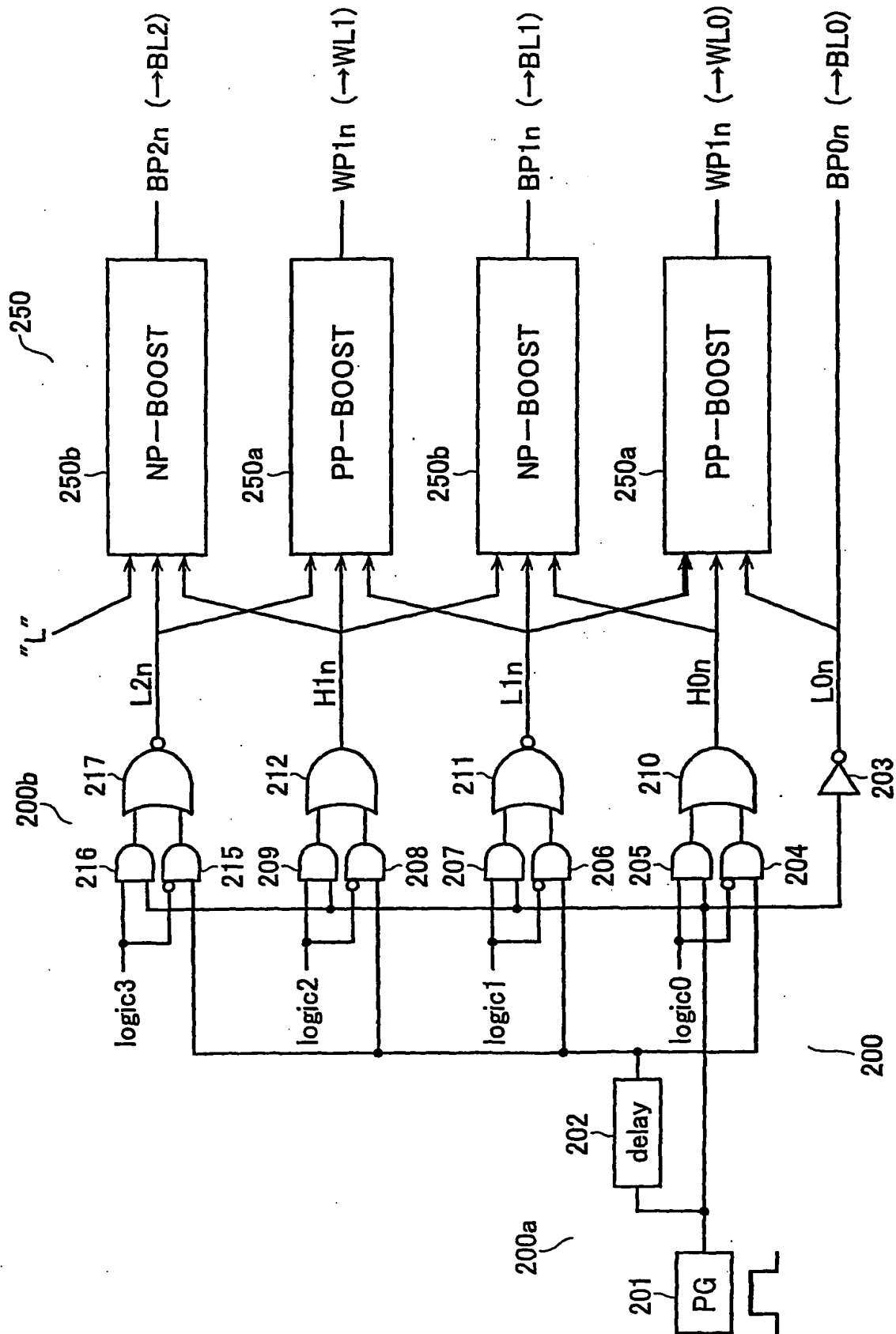






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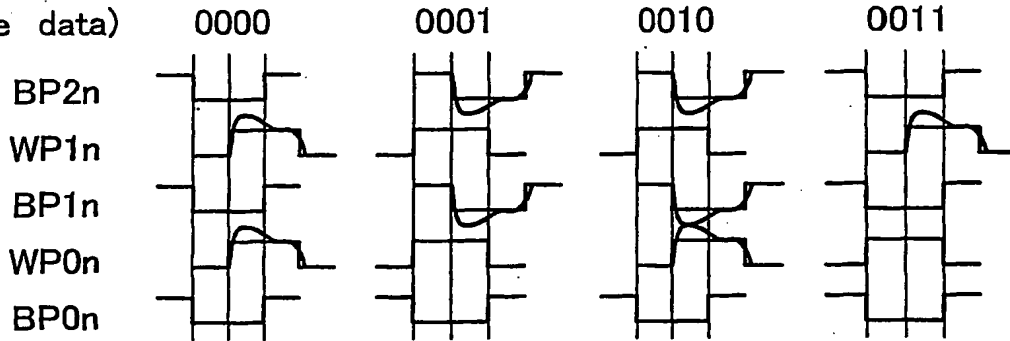
FIG. 65



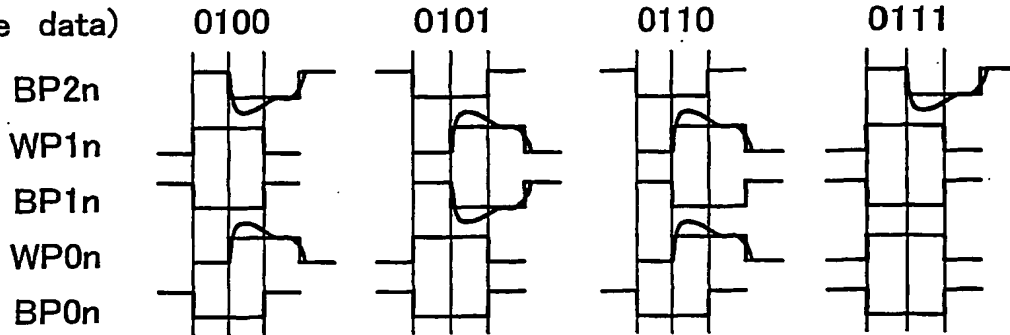
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FIG. 66

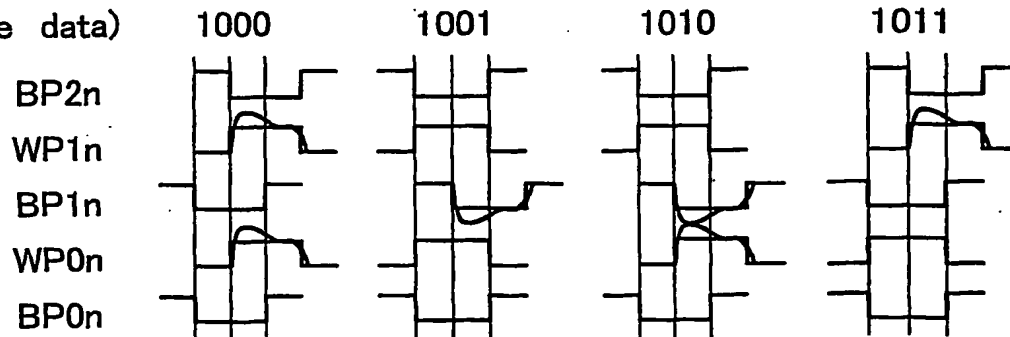
(16-Value data)



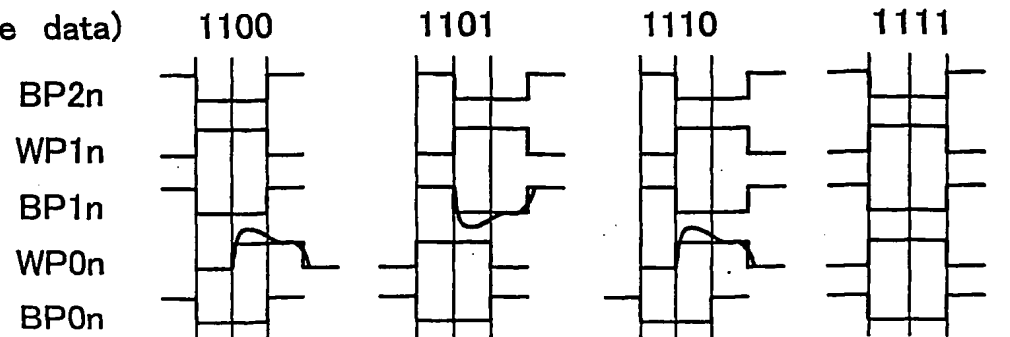
(16-Value data)



(16-Value data)



(16-Value data)



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FIG. 67

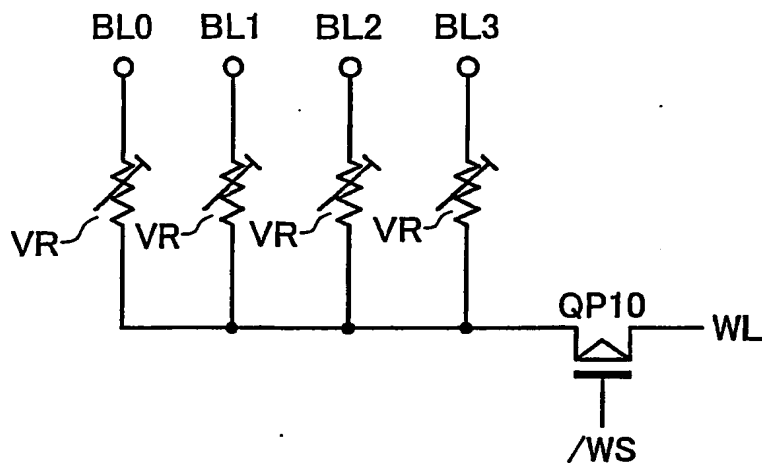
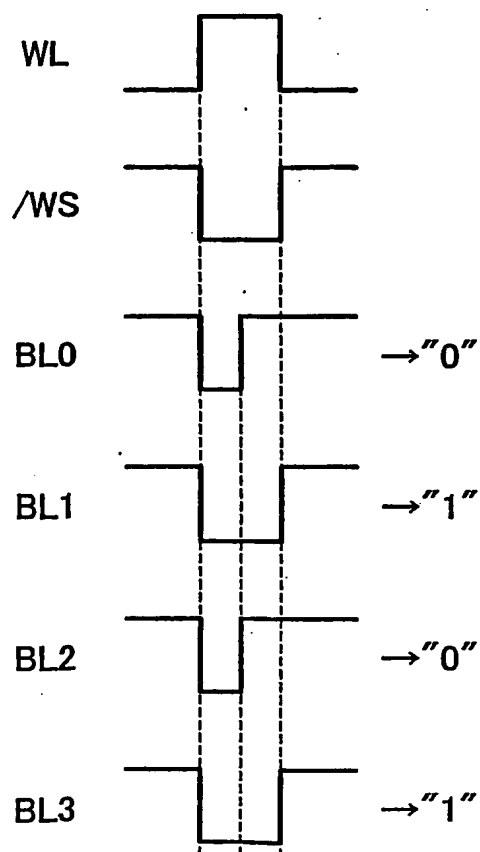
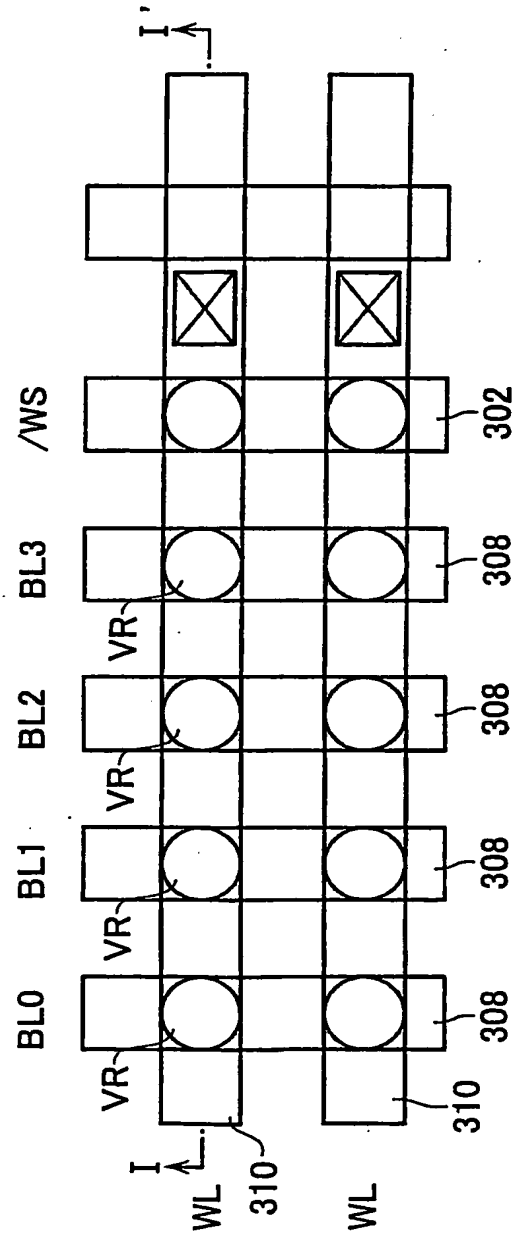


FIG. 68



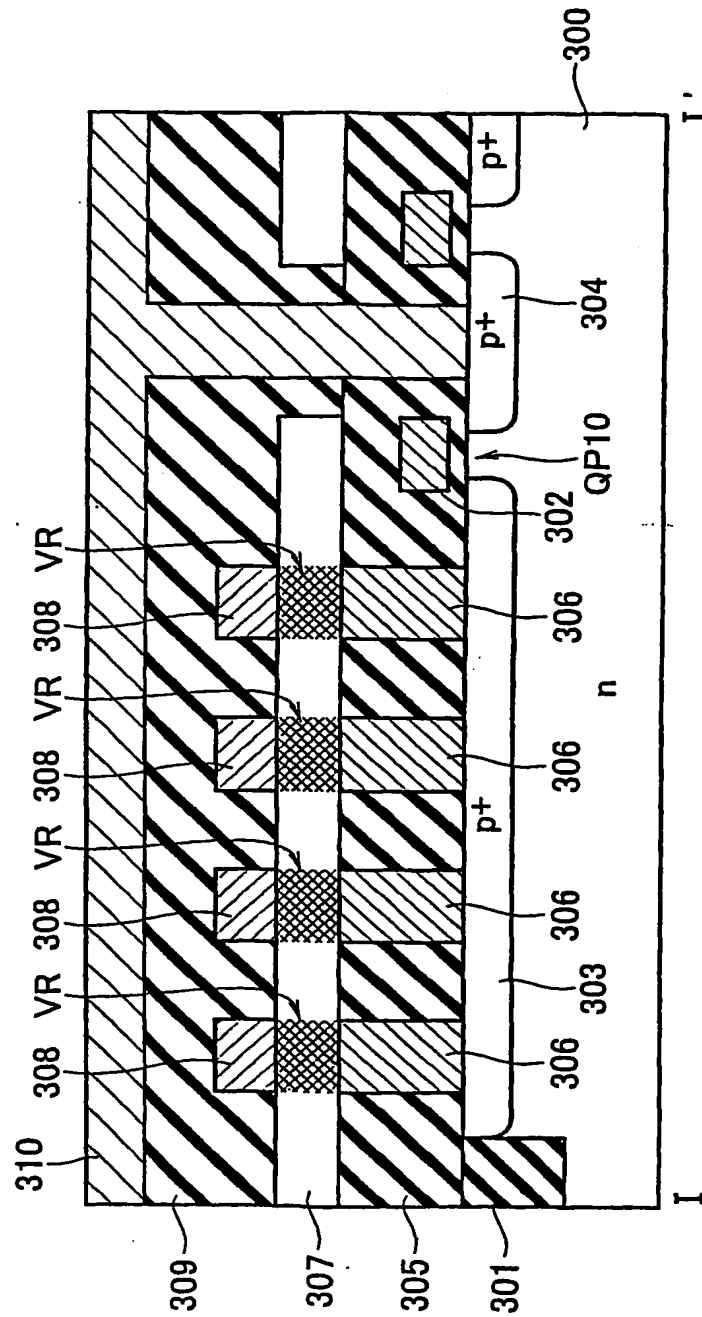
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FIG. 69



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FIG. 70



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FIG. 71

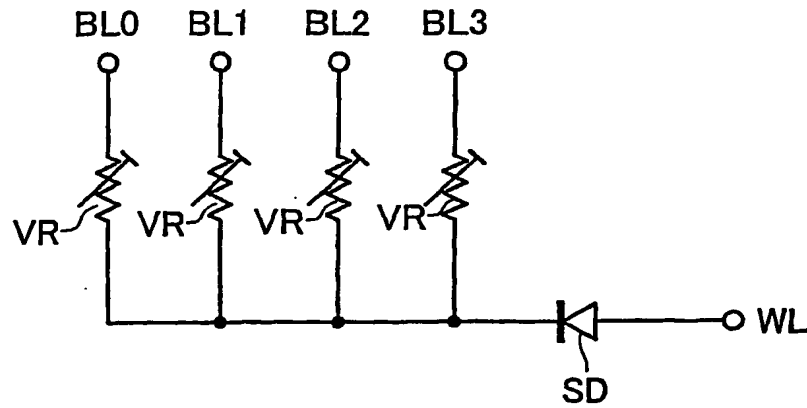


FIG. 72

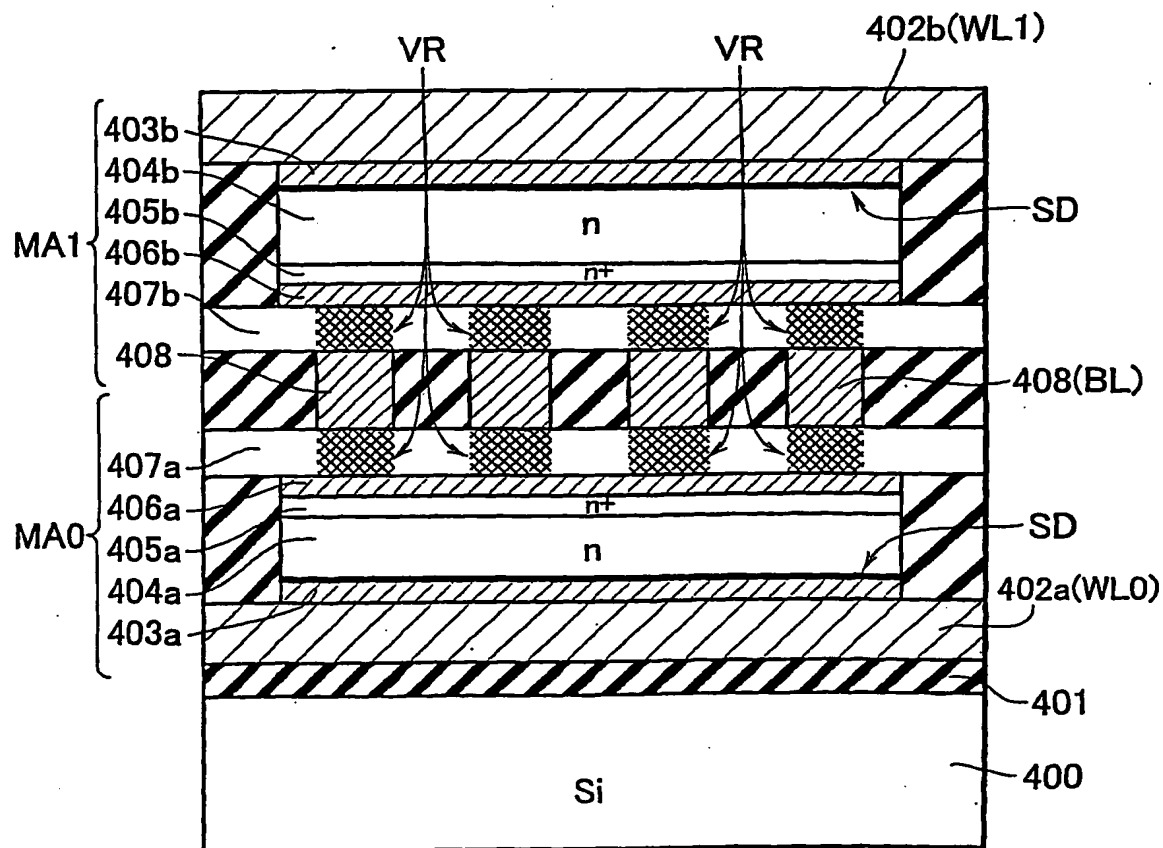


FIG. 73

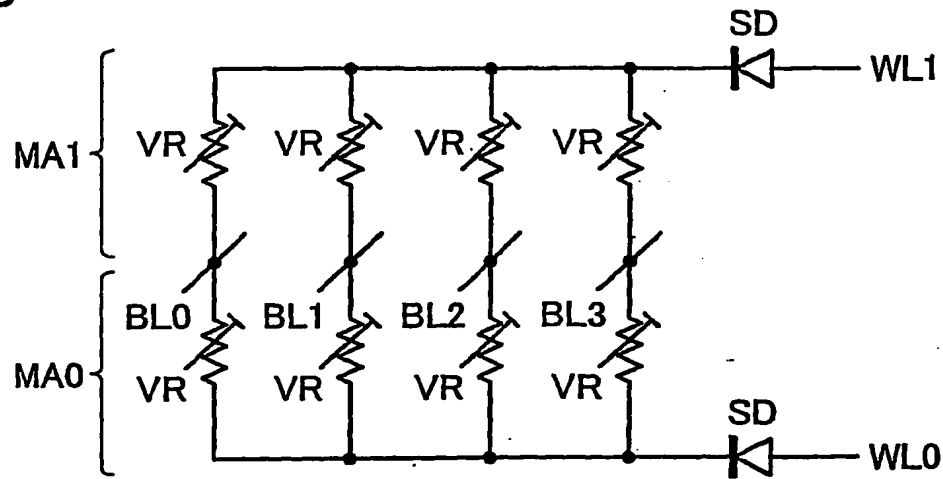


FIG. 74

